SYED AMMAL ENGINEERING COLLEGE

(Approved by the AICTE, New Delhi, Govt. of Tamilnadu and Affiliated to Anna University,Chennai)

Established in 1998 - An ISO 9001:2008 Certified Institution

Dr. E.M.AbdullahCampus,Ramanathapuram – 623 502.

Computer Science and Engineering

CS6303-COMPUTER ARCHITECTURE

UNIT – I

OVERVIEW AND INSTRUCTIONS

PART A

1. Define Computer Architecture
2. Define Computer H/W
3. What are the functions of control unit ?
4. 4.Define Interrupt
5. What are the uses of interrupts?
6. What is the need for reduced instruction chip?
7. Name any three of the standard I/O interface.
8. Differentiate between RISC and CISC
9. Explain the various classifications of parallel structures.
10. What is absolute addressing mode?
11. Specify three types of data transfer techniques.
12. What is the role of MAR and MDR?
13. What are the various types of operations required for instructions?
14. What is the role of IR and PC?
15. 15.What are the various units in the computer?
16. What is an I/O channel?
17. 17.What is a bus?
18. 18.Define word length?
19. 19.Explain the following the address instruction?
20. Zero address instruction.
21. What is the straight-line sequencing?
22. 22.What is the role of PC?
23. Define Signal
24. Define Gates
25. Flip flop
26. 26.State and explain the performance equation?
27. Define CPI
28. 28.Define Throughput and Throughput rate.

PART B

1. Explain the basic functional units
2. Discuss in detail the basic concepts of instructions and its executions
3. Deduce the concept of performance and factors projecting the performance
4. What are addressing modes and enhance the types of addressing modes
5. Design logical and control unit using its instructions

UNIT II

ARITHMETIC OPERATIONS

PART-A

1. State the principle of operation of a carry look-ahead adder.
2. What are the main features of Booth's algorithm?
3. How can we speed up the multiplication process?(CSE Nov/Dec 2003)
4. What is bit pair recoding? Give an example.
5. What is the advantage of using Booth algorithm?
6. Write the algorithm for restoring division.
7. When can you say that a number is normalized?
8. Explain about the special values in floating point numbers.
9. Write the Add/subtract rule for floating point numbers.
10. Write the multiply rule for floating point numbers.
11. What is the purpose of guard bits used in floating point arithmetic
12. What are the ways to truncate the guard bits?
13. Define carry save addition(CSA) process.
14. What are generate and propagate function?
15. What is floating point numbers?
16. In floating point numbers when so you say that an underflow or overflow has occurred?
17. What are the difficulties faced when we use floating point arithmetic?
18. In conforming to the IEEE standard mention any four situations under which a processor sets exception flag.
19. Why floating point number is more difficult to represent and process than integer?(CSE May/June 2007)
20. Give the booth's recoding and bit-pair recoding of the computer.
21. Draw the full adder circuit and give the truth table (CSE May/June 2007)

PART B

1. Explain the Booth's algorithm for multiplication of signed two's complement numbers.
2. Explain the floating point addition and subtraction.
3. State the Non –restoring division technique.
4. Explain with a diagram the design of a fast multiplier using carry save adder circuit.
5. Give the block diagram for a floating point adder and subtractor unit and discuss its operation.
6. Draw and explain the flowchart of floating point addition process.

UNIT III

PROCESSOR AND CONTROL UNIT

PART A

1. Define MIPS .
2. Define MIPS Rate:
3. Define pipelining.
4. Define parallel processing.
5. Define instruction pipeline.
6. What are the steps required for a pipelinened processor to process the instruction?
7. What are Hazards?
8. State different types of hazards that can occur in pipeline.
9. Define Data hazards
10. Define Instruction hazards
11. Define Structural hazards?
12. What are the classification of data hazards?
13. Define RAW hazard : (read after write)
14. Define WAW hazard :(write after write)
15. .Define WAR hazard :(write after read)
16. How data hazard can be prevented in pipelining?
17. How Compiler is used in Pipelining?
18. How addressing modes affect the instruction pipelining?
19. What is locality of reference?
20. What is the need for reduced instruction chip?
21. Define memory access time?
22. Define memory cycle time.
23. Define Static Memories.
24. List out Various branching technique used in micro program control unit?
25. How the interrupt is handled during exception?
26. List out the methods used to improve system performance.

PART B

1. State and explain the different types of hazards that can occur in a pipeline.
2. Draw and explain the structure of a superscalar processor. Also explain the flow of instruction execution in it.
3. Explain the control implemation scheme in detail
4. Implement basic structure of MIPS
5. Define datahazard and instruction hazard and explain in detail
6. Explain pipelined data path and control path
7. What are the two aspects of machine instruction? Explain it .
8. .Draw and explain the modified three-bus structure of the processor suitable for four stage pipelined execution. How this structure is suitable to provide four-stage pipelined execution?

UNIT – IV

PARALLELISAM

PART A

1. Define parallel processing
2. Define multiprocessor system
3. Define parallel processing program
4. What is cluster
5. What is multicore
6. What is CMP and SMP
7. State Amdahl’s law
8. What is the use of Amdahl’s law
9. What is strong scaling
10. What is weak scaling
11. What is SISD
12. What is SIMD
13. What is MISD
14. What is data level parallelis

15. What is hardware multithreading
16. Compare process switch and thread switch
17. Define interleaved or fine grained multithreading
18. Define blocked or coarse grained multithreading
19. What is UMA processor
20. What is NUMA processor

PART B

1. Explain flyn's classification in detail

2. Discuss the principle of hardware multithreading and elaborate its types

3. What are multicore processors and explain it

4. Deduce the challenges faced in parallelism

5. Discuss in detail instruction level parallelism

UNIT – V

MEMORY SYSTEM MEMORY AND I/O SYSTEMS

PART A

1. Give the classification of the Optical Media
2. What is a Mini Disk?
3. List some applications for WORM.
4. What are multifunctional drives
5. What are types of technology used in s multifunctional drive?
6. What is Migration and Archiving?
7. What is the use of High water marks in a cache?
8. What are the various cache usage in a LAN –based system?
9. What are the multimedia applications which use caches?
10. Explain virtual memory technique.
11. What are virtual and logical addresses?
12. Define translation buffer.
13. What is branch delay slot?
14. What is optical memory?

15. What are static and dynamic memories?
16. What are the components of memory management unit?
17. Distinguish Between Static RAM and Dynamic RAM?
18. Distinguish between asynchronies DRAM and synchronous RAM.
19. What do you mean associative mapping technique?
20. What is SCSI?
21. What are the two types of latencies associated with storage?
22. What are the data management activities involved in a storage?
23. What do you mean by Disk Spanning?
24. List some objectives for using RAID Systems
25. What are the different levels RAID?
26. Two Types of storage devices.
27. Explain very briefly about ESDI Hard Drive
28. Explain in brief about IDE
29. Define the term RELIABILITY
30. Define the term AVAILABLITY:
31. How the interrupt is handled during exception?
32. What is IO mapped input output?
33. Specify the three types of the DMA transfer techniques?
34. What is an interrupt?
35. What are the uses of interrupts?
36. Define vectored interrupts.
37. Name any three of the standard I/O interface
38. What is an I/O channel?
39. Why program controlled I/O is unsuitable for high-speed data transfer?
40. what is the function of i/o interface?
41. Name some of the IO devices.
42. What are the steps taken when an interrupt occurs?
43. Define interface.
44. What is programmed I/O?
45. What is DMA?

PART B

1. Define cache memory. Explain the mapping process followed in cache memory. Also discuss
2. the relative advantages and disadvantages of the mapping techniques used.

3. What is virtual memory? Why is it necessary to implement virtual memory? Explain the virtual
4. Explain Memory address translation.
5. Draw and explain the various types of secondary storage devices.
6. List the different types of interrupts. Explain briefly about mask able interrupt.
7. What is DMA? Explain the block diagram of DMA .Also describe how DMA is used to
8. Explain Transfer data from peripherals.
9. Expalin input/output processors