VLSI DESIGN

1. NMOS devices are formed in
a) p-type substrate of high doping level
b) n-type substrate of low doping level
c) p-type substrate of moderate doping level
d) n-type substrate of high doping level

Answer: c
Explanation: nMOS devices are formed in a p-type substrate of moderate doping level. nMOS devices have higher mobility and is cheaper.

2.Source and drain in nMOS device are isolated by
a) a single diode
b) two diodes
c) three diodes
d) four diodes

Answer: b
Explanation: The source and drain regions are formed by diffusing n-type impurity, it gives rise to depletion region which extend in more lightly doped p-region. Thus Source and drain in a nMOS device are isolated by two diodes.

3. In depletion mode, source and drain are connected by
a) insulating channel
b) conducing channel
c) Vdd
d) Vss

Answer: b
Explanation: In depletion mode, source and drain are connected by conducting channel but the channel can be closed by applying suitable negative voltage to the gate.

4. The condition for non saturated region is
a) Vds = Vgs – Vt
b) Vgs lesser than Vt
c) Vds lesser than Vgs – Vt
d) Vds greater than Vgs – Vt

Answer: c
Explanation: The condition for non saturated region is Vds lesser Vgs – Vt. In non saturation region MOSFET acts as voltage source. Varying Vds will provide significant change in drain current.

5. In enhancement mode, device is in_____condition
a) conducting
b) non conducting
c) partially conducting
d) insulating

Answer: b
Explanation: In enhancement mode, the decive is in non conducting condition. For n-type FET, thershold voltage is positive and p-type threshold voltage is negative.

6. The condition for non conducting mode is
a) Vds lesser than Vgs
b) Vgs lesser than Vds
c) Vgs = Vds = 0
d) Vgs = Vds = Vs = 0

Answer: d
Explanation: In enhancement mode the device is in non conducting mode, and its condition is Vds = Vgs = Vs = 0.

7. nMOS is
a) donor doped
b) acceptor doped
c) all of the mentioned
d) none of the mentioned

Answer: b
Explanation: nMOS transistors are acceptor doped. Acceptor is a dopant which when added forms p-type region. Some of the accpetors are silicon, boron, aluminium etc.

8. MOS transistor structure is
a) symmetrical
b) non symmetrical
c) semi symmetrical
d) pseudo symmetrical

Answer: a
Explanation: MOS transistor structure is completely symmetrical with respect to source and drain.

9.. pMOS is
a) donor doped
b) acceptor doped
c) all of the mentioned
d) none of the mentioned

Answer: a
Explanation: nMOS is acceptor doped and pMOS is donor doped devices. Acceptor doped forms p-type region and donor doped forms n-type region.

10. Inversion layer in enhancement mode consists of excess of
a) positive carriers
b) negative carriers
c) both in equal quantity
d) neutral carriers

Answer: b
Explanation: Inversion layer in enhancement mode consists of excess of negative carriers that is electron.

11. The condition for linear region is
a) Vgs lesser than Vt
b) Vgs greater than Vt
c) Vds lesser than Vgs
d) Vds greater than Vgs

Answer: b
Explanation: The condition for linear region is Vgs > Vt. The power of MOS in linear region is less. It is a power dissipating region.

12. As source drain voltage increases, channel depth
a) increases
b) decreases
c) logarithmically increases
d) exponentially increses

Answer: b
Explanation: As source drain voltage Vds increases, the channel depth at the drain end decreases.

13. Speed power product is measured as the product of
a) gate switching delay and gate power dissipation
b) gate switching delay and gate power absorption
c) gate switching delay and net gate power
d) gate power dissipation and absorption

Answer: a
Explanation: Speed power product is measure in picojoules and it is the product of gate switching delay and gate power dissipation.

MOS TRANSISTORS

1. MOS transistors consists of
a) semiconductor layer
b) metal layer
c) layer of silicon-di-oxide
d) all of the mentioned

Answer: d
Explanation: MOS transistors is formed as a sandwich consisting of a semiconductor layer, a silicon-di-oxide layer and a metal layer.

2. In MOS transistors,_____is used for their gate
a) metal
b) silicon-di-oxide
c) polysilicon
d) gallium

Answer: c
Explanation: In MOS transistors, polycrystalline silicon is used for their gate region instead of metal. Polysilicon gates have replaced all other older devices.

3. The gate region consists of
a) insulating layer
b) conducting layer
c) lower metal layer
d) p type layer

Answer: b
Explanation: The gate region is a sandwich consisting of semiconductor layer, an insulating layer and an upper metal layer.

4. Electrical charge flows from
a) source to drain
b) drain to source
c) source to ground
d) source to gate

Answer: a
Explanation: Electrical charge or current flows from source to drain depending on the charge applied to the gate region.

5. Source in MOS transistors is doped with_____material
a) n-type
b) p-type
c) n & p type
d) none of the mentioned

Answer: a
Explanation: Source and drain in the MOS transistors are doped with N-type material and substrate is doped with p-type material.

6. In N channel MOSFET which is the more negative of the elements?
a) source
b) gate
c) drain
d) source and drain

Answer: a
Explanation: In N channel MOSFET, source is the more negative of the elements and in the case of P channel MOSFET, it is the more positive of the elements.

7. If the gate is given sufficiently large charge, electrons will be attracted to
a) drain region
b) channel region
c) switch region
d) bulk region

Answer: b
Explanation: If the gate is given sufficiently large charge, the negative charge carreirs, electrons will be attracted from the bulk of the substrate material into the channel region below the oxide.

8. Enhancement mode device acts as_____switch, depletion mode acts as _____switch
a) open, closed
b) closed, open
c) open, open
d) close, close

Answer: a
Explanation: Enhancement mode transistor acts as open switch whereas depletion mode transistor acts as normally closed switch.

9. Depletion mode MOSFETs are more commonly used as
a) switches
b) resistors
c) buffers
d) capacitors

Answer: b
Explanation: Depletion mode MOSFETs are more commonly used as resistors than as switches. As permanently on switch it has high resistance.

10. Enhancement mode MOSFETs are more commonly used as
a) switches
b) resistors
c) buffers
d) capacitors

Answer: a
Explanation: Enhancement mode MOSFETs are more commonly used as switches and depletion mode devices are more used as resistors.

11. Depletion mode transistor should be large.
a) true
b) false

Answer: a
Explanation: Depletion mode transistors should be made large that is long and thin to create the large ‘on’ resistance.

12. Which expression is true?
a) charging time < discharging time
b) charging time > discharging time
c) charging time = discharging time
d) charging time and discharging time are not related

Answer: b
Explanation: When driving a capacitive output load, charging time will be long compared to the discharging time.

13. Overheating in device occurs due to less number of resistors per unit area.
a) true
b) false

Answer: b
Explanation: When the number of resistors per unit area increases, the device may not dissipate heat very well. This results in device overheating which leads to its failure.

14. In n channel MOSFET,_____is constant
a) channel length
b) channel width
c) channel depth
d) channel concentration

Answer: a
Explanation: In all n channel MOSFET transistors, channel length is constant where as channel width can be varied.

VLSI Design

1. VLSI technology uses_____to form integrated circuit
a) transistors
b) switches
c) diodes
d) buffers

Answer: a
Explanation: Very-large scale integration is the process of creating integrated circuit with thousands of transistors into one single chip.

2. Medium scale integration has
a) ten logic gates
b) fifty logic gates
c) hundred logic gates
d) thousands logic gates

Answer: c
Explanation: Small scale integration has one or more logic gate. Further improved technology is medium scale integration which consists of hundred logic gates. Large scale integration has thousand logic gates.

3. The difficulty in achieving high doping concentration leads to
a) error in concentration
b) error in variation
c) error in doping
d) distrubution error

Answer: b
Explanation: As photolithography comes closer to fundamental law of optics, achieving high accuracy in doping concentration becomes difficult, which leads to error due to variation.

4. _____is used to deal with effect of variation
a) chip level technique
b) logic level technique
c) switch level technique
d) system level technique

Answer: d
Explanation: Designers must simulate multiple fabrication process or use system level technique for dealing with effects of variation.

5. As die size shrinks, the complexity of making the photomasks
a) increases
b) decreases
c) remains the same
d) cannot be determined

Answer: a
Explanation: As the die size shrinks due to scaling, the number of die per wafer increases and the complexity of making the photomasks increases rapidly.

6. _____architecture is used to design VLSI
a) system on a device
b) single open circuit
c) system on a chip
d) system on a circuit

Answer: c
Explanation: SoC that is system on a chip architecture is used to design the very high level integrated circuit.

7. The design flow of VLSI system is
1. architecture design 2. market requirement 3. logic design 4. HDL coding
a) 2-1-3-4
b) 4-1-3-2
c) 3-2-1-4
d) 1-2-3-4

Answer: a
Explanation: The order of the design flow of VLSI circuit is market requirement, architecture design, logic design, HDL coding and then verification.

8. _____is used in logic design of VLSI
a) LIFO
b) FIFO
c) FILO
d) LILO

Answer: b
Explanation: First in first out (FIFO) technique and finite state machine technique is used in the logic design of the VLSI circuits.

9. Which provides higher integration density?
a) switch transistor logic
b) transistor buffer logic
c) transistor transistor logic
d) circuit level logic

Answer: c
Explanation: Transistor-transistor logic offers higher integration density and it became the first integrated circuit revolution.

10. Physical and electrical specification is given in
a) architectural design
b) logic design
c) system design
d) functional design

Answer: d
Explanation: Functional design defines the major functional units of the system, interconnections, physical and electrical specifications.

11. Which is the high level representation of VLSI design
a) problem statement
b) logic design
c) HDL program
d) functional design

Answer: a
Explanation: Problem statement is a high level representation of the system. Performance, functionality and physical dimensions are considered here.

12. Gate minimization technique is used to simplify the logic.
a) true
b) false

Answer: a
Explanation: Gate minimization technique is used to find the simplest, smallest and effective implementation of the logic.

NMOS Fabrication

1. nMOS fabrication process is carried out in
a) thin wafer of a single crystal
b) thin wafer of multiple crystals
c) thick wafer of a single crystal
d) thick wafer of multiple crystals

Answer: a
Explanation: nMOS fabrication process is carried out in thin wafer of a single crystal with high purity.

2. _____impurities are added to the wafer of the crystal
a) n impurities
b) p impurities
c) siicon
d) crystal

Answer: b
Explanation: p impurities are introduced as the crystal is grown. This increases the hole concentration in the device.

3. What kind of substrate is provided above the barrier to dopants?
a) insulating
b) conducting
c) silicon
d) semi conducting

Answer: a
Explanation: Above a layer of silicon dioxide which acts as barrier, insulating layer is provided upon which other layers may be deposited and patterned.

4. The photoresist layer is exposed to
a) visible light
b) ultraviolet light
c) infra red light
d) LED

Answer: b
Explanation: The photoresist layer is exposed to ultraviolet light to mark the regions where diffusion is to take place.

5. In nMOS device, gate material could be
a) silicon
b) polysilicon
c) boron
d) phosporus

Answer: b
Explanation: In nMOS device, the gate material could be metal or polysilicon. This polysilicon layer has heavily doped polysilicon deposited by CVD.

6. The commonly used bulk substrate in nMOS fabrication is
a) silicon crystal

b) silicon-on-sapphire
c) phosporus
d) silicon-di-oxide

Answer: c
Explanation: In nMOS fabrication, the bulk substrate used can be either bulk silicon or silicon-on-sapphire.

7. In nMOS fabrication, etching is done using
a) plasma
b) hydrochloric acid
c) sulphuric acid
d) sodium chloride

Answer: a
Explanation: In nMOS fabrication, etching is done using hydroflouric acid or plasma. Etching is a process used to remove layers from the surface.

8. Heavily doped polysilicon is deposited using
a) chemical vapour decomposition
b) chemical vapour deposition
c) chemical deposition
d) dry deposition

Answer: b
Explanation: The polysilicon layer consists of heavily doped polysilicon deposited by chemical vapour deposition.

9. In diffusion process,_____impurity is desired
a) n type
b) p type

Answer: a
Explanation: Diffusion is carried out by heating the wafer to high temperature and passing a gas containing the desired ntype impurity.

10. Contact cuts are made in
a) source
b) drain
c) metal layer
d) diffusion layer

Answer: a
Explanation: Contact cuts are made in the desired polysilicon area, source and gate. COntact cuts are those places where connection has to be made.

11. Interconnection pattern is made on
a) polysilicon layer
b) silicon-di-oxide layer
c) metal layer
d) diffusion layer

Answer: c
Explanation: The metal layer is masked and etched to form interconnection pattern. The metal layer was formed using aluminium deposited over the formed surface.

12. SIlicon-di-oxide is a good insulator.
a) true
b) false

Answer: a
Explanation: SIlicon-di-oxide is a very good insulator so a very thin layer is required in the fabrication of MOS transistor.

13. _____is used to suppress unwanted conduction
a) phosporus
b) boron
c) silicon
d) oxygen

Answer: b
Explanation: Boron is used to suppress the unwanted conduction between transistor sites. It is implanted in the exposed regions.

14. Which is used for the interconnection?
a) boron
b) oxygen
c) aluminium
d) silicon

Answer: c
Explanation: Aluminium is the suitable material used for the circuit interconnection or connecting two layers.

CMOS Fabrication

1. CMOS technology is used in developing
a) microprocessors
b) microcontrollers
c) digital logic circuits
d) all of the mentioned

Answer: d
Explanation: CMOS technology is used in developing microcontrollers, microprocessors, digital logic circuits and other integrated circuits.

2. CMOS has
a) high noise margin
b) high packing density
c) high power dissipation
d) high complexity

Answer: b
Explanation: Some of the properties of CMOS are that it has low power dissipation, high packing density and low noise margin.

3. In CMOS fabrication, nMOS and pMOS are integrated in same substrate.
a) true
b) false

Answer: a
Explanation: In CMOS fabrication, nMOS and pMOS are integrated in the same chip substrate. n-type and p-type devices are formed in the same structure.

4. P-well is created on
a) p subtrate
b) n substrate
c) p & n substrate
d) none of the mentioned

Answer: b
Explanation: P-well is created on n substrate to accommodate n-type devices whereas p-type devices are formed in the ntype substrate.

5. Oxidation process is carried out using
a) hydrogen
b) low purity oxygen
c) sulphur
d) nitrogen

Answer: a
Explanation: Oxidation process is carried out using high purity oxygen and hydrogen. Oxidation is a process of oxidizing or being oxidised.

6. Photo resist layer is formed using
a) high sensitive polymer
b) light sensitive polymer
c) polysilicon
d) silicon di oxide

Answer: b
Explanation: Light sensitive polymer is used to form the photoresist layer. Photoresist is a light sensitive material used to form patterned coating on a surface.

7. In CMOS fabrication,the photoresist layer is exposed to
a) visible light
b) ultraviolet light
c) infra red light
d) fluorescent

Answer: b
Explanation: The photoresist layer is exposed to ultraviolet light to mark the regions where diffusion is to take place.

8. Few parts of photoresist layer is removed by using
a) acidic solution
b) neutral solution
c) pure water
d) diluted water

Answer: a
Explanation: Few parts of photoresist layer is removed by treating the wafer with basic or acidic solution. Acidic solutions are those which have pH less than 7 and basic solutions have greater than 7.

9. P-well doping concentration and depth will affect the
a) threshold voltage
b) Vss
c) Vdd
d) Vgs

Answer: a
Explanation: Diffusion should be carried out very carefully, as doping concentration and depth will affect both threshold voltage and breakdown voltage.

10. Which type of CMOS circuits are good and better?
a) p well
b) n well
c) all of the mentioned
d) none of the mentioned

Answer: b
Explanation: N-well CMOS circuits are better than p-well CMOS circuits because of lower substrate bias effect.

11. N-well is formed by
a) decomposition
b) diffusion
c) dispersion
d) filtering

Answer: b
Explanation: N-well is formed by using ion implatation or diffusion. Ion implantation is a process by which ions of a material are accelerated in an electrical field and impacted into a solid. Diffusion is a process in which net movement of ions or molecules play a major role.

12. _____is sputtered on the whole wafer
a) silicon
b) calcium
c) potassium
d) aluminium

Answer: d
Explanation: Aluminium is sputtered on the whole waffer before removing the excess metal from the wafer.

1. MOS technology has more load driving capability.
a) true
b) false

Answer: b
Explanation: One of the disadvantage of MOS technology is it has limited load driving capabilities.

2. What is the disadvantage of MOS device?
a) limited current sourcing
b) limited voltage sinking
c) limited voltage sourcing
d) unlimited current sinking

Answer: a
Explanation: MOS devices have limited current sourcing and current sinking abilities.

3. What are the advantages of BiCMOS?
a) higher gain
b) high frequency characteristics
c) better noise characteristics
d) all of the mentioned

Answer: d
Explanation: BiCMOS provides higher gain, better noise and high frequency characteristics than MOS transistors.

4. What are the features of BiCMOS ?
a) low input impedance
b) high packing density
c) high input impedance
d) bidirectional

Answer: a
Explanation: Some of the features of BiCMOS are low input impedance, low packing density, unidirectional, high output drive current etc.

5. BiCMOS has low power dissipation.
a) true
b) false

Answer: b
Explanation: BiCMOS has high power dissipation and CMOS has low power dissipation.

6. CMOS is
a) unidirectional
b) bidirectional
c) directional
d) none of the mentioned

Answer: a
Explanation: BiCMOS is unidirectional and CMOS is bidirectional.

7. In bipolar transistor, its quality can be improved by
a) increasing collector resistance
b) decreasing collector resistance
c) collector resistance does not affect the quality
d) decreasing gate resistance

Answer: b
Explanation: The quality of bipolar transistor can be improved by reducing the collector resistance, which can be done by using the additional layer of n+ subcollector.

8. BiCMOS can be used in
a) amplifyig circuit
b) driver circuits
c) divider circuit
d) multiplier circuit

Answer: b
Explanation: BiCMOS is more advantageous and improved than CMOS and it can be used in I/O and driver circuits.

9. Advantages of E-beam masks are
a) small feature size
b) larger feature size
c) looser layer
d) complex design

Answer: a
Explanation: The advantages of E-beam masks are it has tighter layer to layer registration and it has smaller feature sizes.

10. Which process is used in E-beam machines?
a) raster scanning
b) vector scanning
c) both of the mentioned
d) none of the mentioned

Answer: c
Explanation: The two approaches to the design of E-beam machines are raster scanning and vector scanning.

11. What is the feature of vector scanning?
a) faster
b) slow
c) easy handling
d) very simple design

Answer: a
Explanation: Vector scanning is faster but data handling involved is more complex. Vector scanning is done between the end points.

12. Which has high input resistance?
a) nMOS
b) CMOS
c) pMOS
d) BiCMOS

Answer: b
Explanation: CMOS technology has high input resistance and is best for constructing simple low-power logic gates.

13. BiCMOS has lower standby leakage current.
a) true
b) false

Answer: b
Explanation: BiCMOS has potential for high standby leakage current and has high power consumption compared to CMOS.

VLSI Questions and Answers – NMOS and CMOS Fabrication

1. Lithography is:
a) Process used to transfer a pattern to a layer on the chip
b) Process used to develop an oxidation layer on the chip
c) Process used to develop a metal layer on the chip
d) Process used to produce the chip

Answer: a
Explanation: Lithography is the process used to develop a pattern to a layer on the chip.

2. Silicon oxide is patterned on a substrate using:
a) Physical lithography
b) Photolithography
c) Chemical lithography
d) Mechanical lithography

Answer: b
Explanation: Silicon oxide is patterned on a substrate using Photolithography.

3. Positive photo resists are used more than negative photo resists because:
a) Negative photo resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the positive photo resists
b) Positive photo resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the negative photo resists
c) Negative photo resists are less sensitive to light
d) Positive photo resists are less sensitive to light

Answer: a
Explanation: Negative photo resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the positive photo resists. Therefore, negative photo resists are-used less commonly in the manufacturing of high-density integrated circuits.

4. The_____is used to reduce the resistivity of poly silicon:
a) Photo resist
b) Etching
c) Doping impurities
d) None of the mentioned

Answer: c
Explanation: The resistivity of poly silicon is reduced by Doping impurities.

5. The isolated active areas are created by technique known as:
a) Etched field-oxide isolation
b) Local Oxidation of Silicon
c) Both the mentioned
d) None of the mentioned

Answer: c
Explanation: To create isolated active areas both the techniques can be used. Among them Local Oxidation of Silicon(LOCOS) is most efficient.

6. The chemical used for shielding the active areas to achieve selective oxide growth is:
a) Silver Nitride
b) Silicon Nitride
c) Hydrofluoric acid
d) Polysilicon

Answer: b
Explanation: Selective oxide growth is achieved by shielding the active areas. Silicon nitride (Si3N4) is used for shielding the active areas during oxidation, which effectively inhibits oxide growth.

7. The dopants are introduced in the active areas of silicon by:
a) Diffusion process
b) Ion Implantaion process
c) Chemical Vapour Deposition
d) Either Diffusion or Ion Implantaion Process

Answer: d
Explanation: Two ways to add dopants are diffusion and ion implantation.

8. To grow the polysilicon gate layer, the chemical used for chemical vapour deposition is:
a) Silicon Nitride(Si4N3)
b) Silane gas(SiH4)
c) Silicon oxide
d) None of the mentioned

Answer: b
Explanation: Silicon Wafer is placed in a reactor with silane gas (SiH4), and they are heated again to grow the polysilicon layer by chemical vapor deposition.

9. The process by which Aluminium is grown over the entire wafer , also filling the contact cuts is:
a) Sputtering
b) Chemical vapour deposition
c) Epitaxial growth
d) Ion Implantation

Answer: a
Explanation: Aluminum is sputtered over the entire wafer, it also fills the contact cuts.

10. Chemical Mechanical Polisihing is used to:
a) Remove silicon oxide
b) Remove silicon nitride and pad oxide
c) Remove polysilicon gate layer
d) Reduce the size of the layout

Answer: b
Explanation: The pad oxide and nitride are removed using a Chemical Mechanical Polishing (CMP) step.

12. Gate oxide layer consists of:
a) SiO2 layer, overlaid with a few layers of an oxynitrided oxide
b) Only SiO2 Layer
c) SiO2 layer with Polysilicon Layer
d) SiO2 layer and stack of epitaxial layers of Polysilicon

Answer: a
Explanation:Current processes seldom use a pure SiO2 gate oxide, but prefer to produce a stack that consists of a few atomic layers, each 3–4 Å thick, of SiO2 for reliability, overlaid with a few layers of oxy-nitrided oxide (one with nitrogen added).

13. What is Piranha Solution
a) It is a 3:1 to 5:1 mix of nitric acid and hydrogen peroxide that is used to develop the oxide layer on silicon substrate
b) It is a 3:1 to 5:1 mix of sulphuric acid and hydrofluoric acid that is used to clean silicon wafers removing organic and metal contaminants or photo resist after metal patterning
c) It is a 3:1 to 5:1 mix of sulphuric acid and hydrogen peroxide that is used to grow the oxide layer on the silicon
d) It is a 3:1 to 5:1 mix of sulphuric acid and hydrogen peroxide that is used to clean wafers of organic and metal contaminants or photo resist after metal patterning

Answer: d
Explanation: Piranha solution is a 3:1 to 5:1 mix of sulfuric acid and hydrogen-peroxide that is used to clean silicon wafers of metal and organic contaminants or photo-resist after metal patterning.

Ids versus Vds Relationships

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "Ids versus Vds Relationships".

1. Ids depends on
a) Vg
b) Vds
c) Vdd
d) Vss

Answer: b
Explanation: Ids depends on both Vgs and Vds. The charge induced is dependent on gate to source voltage Vgs also charge can be moved from source to drain under influence of electric field created by Vds.

2. Ids can be given by
a) Qc x Ƭ
b) Qc / Ƭ
c) Ƭ / Qc
d) Qc / 2Ƭ

Answer: b
Explanation: Ids can be given as charge induced in the channel(Qc) divided by transit time (Ƭ). Ids is equivalent to (-Isd).

3. Transit time can be given by
a) L / v
b) v / L
c) v x L
d) v x d

Answer: a
Explanation: Transit time (Ƭ) can be given by lenght of channel(L) by velocity(v). Transit time is the time required for an electron to travel between two electrodes.

4. Velocity can be given as
a) μ / Vds
b) μ / Eds
c) μ x Eds
d) Eds / μ

Answer: b
Explanation: Velocity can be given as the product of electron or hole mobility(μ) and electric field(Eds). It gives the flow velocity which an electron attains due to electric field.

5. Eds is given by
a) Vds / L
b) L / Vds
c) Vds x L
d) Vdd / L

Answer: a
Explanation: Electric field(Eds) can be given as the ratio of Vds and L. Eds is the electric field created from drain to source due to volta Vds.

6. Mobility of proton or hole at room temperature is
a) 650 cm2/V sec
b) 260 cm2/V sec
c) 240 cm2/V sec
d) 500 cm2/V sec

Answer: c
Explanation: The value of mobility of proton or hole at room temperature is 240 cm2/V sec. This gives the measure of how fast an electron can move.

7. In resistive region
a) Vds greater than (Vgs – Vt)
b) Vds lesser than (Vgs – Vt)
c) Vgs greater than (Vds – Vt)
d) Vgs lesser than (Vds – Vt)

Answer: b
Explanation: In non saturated or resistive region, Vds lesser than Vgs – Vt where Vds is the voltage between drain and source, Vgs is the gate-source voltage and Vt is the threshold voltage.

8. The condition for saturation is
a) Vgs = Vds

b) Vds = Vgs – Vt
c) Vgs = Vds – Vt
d) Vds greater than Vgs – Vt

Answer: b
Explanation: The condition for saturation is Vds = Vgs – Vt, since at this point IR drop in the channel equals the effective gate to channel voltage at the drain.

9. Threshold voltage is negative for
a) nMOS depletion
b) nMOS enhancement
c) pMOS depletion
d) pMOS enhancement

Answer: a
Explanation: The threshold voltage for nMOS depletion denoted as Vtd is negative.

10. The current Ids_____as Vds increases
a) increases
b) decreases
c) remains fairly constant
d) exponentially increases

Answer: c
Explanation: The current Ids remains fairly constant as Vds increases in the saturation region.

11. In linear region,_____channel exists
a) uniform
b) non-uniform
c) wide
d) uniform and wide

Answer: a
Explanation: In linear region of MOSFET, the channel is uniform and narrow. This is the concentration distribution.

12. When the channel pinches off?
a) Vgs>Vds
b) Vds>Vgs
c) Vds>(Vgs-Vth)

d) Vgs>(Vds-Vth)

Answer: c
Explanation: In MOSFET, in saturation region, when Vds > (Vgs – Vth), the channel pinches off that is the channel current at the drain spreads out.

13. When threshold voltage is more, leakage current will be
a) more
b) less
c) all of the mentioned
d) none of the mentioned

Answer: b
Explanation: Increasing the threshold voltage, leads to small leakage current when turned off and reduces current flow when turned on.

14. MOSFET is used as
a) current source
b) voltage source
c) buffer
d) divider

Answer: a
Explanation: MOSFET is used as current source. Bipolar junction transistor also acts as good current source.

Parameters of MOS Transistors

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Parameters of MOS Transistors”.

1. The work function difference is neagative for
a) silicon substrate
b) polysilicon gate
c) both of the mentioned
d) none of the mentioned

Answer: c
Explanation: The work function difference between gate and Si (Φms) is negative for silicon substrate and polysilicon gate.

2. Substrate bias voltage is positive for nMOS.
a) true
b) false

Answer: b
Explanation: Substrate bias voltage Vsb is positive for pMOS and negative for nMOS.

3. According to body effect, substrate is biased with respect to
a) source
b) drain
c) gate
d) Vss

Answer: a
Explanation: According to body effect, substrate is biased with respect to the source. Body effect can be seen as a change in the threshold voltage.

4. Increasing Vsb,_____the threshold voltage
a) does not effect
b) decreases
c) increases
d) exponentially increases

Answer: c
Explanation: Increasing the substrate bias voltage Vsb, increases the threshold voltage because it depletes the channel of charge carriers.

5. Transconductance gives the relationship between
a) input current and output voltage
b) output current and input voltage
c) input current and input voltage
d) output current and output voltage

Answer: b
Explanation: Transconductance expresses the relationship between output current Ids and input voltage Vgs.

6. Transconductance can be increased by
a) decreasing the width
b) increasing the width
c) increasing the length

d) decreasing the length

Answer: b
Explanation: Transconductance gm of a MOS device can be increased by increasing its width and it does not depend on length.

7. Increasing the transconductance
a) increases input capacitance
b) decreasing area occupied
c) decreasing input capacitance
d) decrease in output capacitance

Answer: a
Explanation: Increasing the transconductance gm results in increase in input capacitance and area occupied as it is directly proportional.

8. Ids is_____to length L of the channel
a) directly proportional
b) inversely proportional
c) not related
d) logarithmically related

Answer: b
Explanation: Ids is inversely proportional to the length L of the channel and using this relationship strong dependence of output conductance on channel length can be demonstrated.

9. Switching speed of a MOS device depends on
a) gate voltage above threshold
b) carrier mobility
c) length channel
d) all of the mentioned

Answer: d
Explanation: Switching speed of a MOS device depends on gate voltage above threshold and on carrier mobility and inversely as the square of channel length.

10. A fast circuit requires
a) high gm
b) low gm
c) does not depend on gm
d) low cost

Answer: a
Explanation: A fast circuit requires gm as high as possible as the switching speed depends on gate voltage above threshold and on carrier mobility and inversely to square of channel length.

11. Surface mobility depends on
a) effective drain voltage
b) effective gate voltage
c) channel length
d) effective source voltage

Answer: b
Explanation: Surface mobility is dependent on the effective gate voltage (Vgs-Vt). Electron mobility on oriented n-type inversion layer surface is larger than that on a oriented surface.

12. MOS transistor is a
a) minority carrier device
b) majority carrier device
c) majority & minority carrier device
d) none of the mentioned

Answer: b
Explanation: MOS transistor is a majority carrier device,in which current in a conducting channel between the source and drain is modulated by a voltage.

13. The MOS transistor is non conducting when
a) zero source bias
b) zero threshold voltage
c) zero gate bias
d) zero drain bias

Answer: c
Explanation: The MOS transistor normally is at cut-off or becomes non-conducting with zero gate bias (gate voltage-source voltage).

nMOS Inverter

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “nMOS Inverter”.

1. Inverters are essential for
a) NAND gates

b) NOR gates
c) sequential circuits
d) all of the mentioned

Answer: d
Explanation: Inverters are needed for restoring logic levels for NAND and NOR gates, sequential and memory circuits.

2. In basic inverter circuit,_____is connected to ground
a) source
b) gates
c) drain
d) resistance

Answer: a
Explanation: A basic inverter circuit consists of transistor with source connected to ground and a load resistor connected from drain to positive supply rail Vdd.

3. In inverter circuit,_____transistors is used as load
a) enhancement mode
b) depletion mode
c) all of the mentioned
d) none of the mentioned

Answer: b
Explanation: Depletion mode transistors are preferred to be used as load in inverter circuits as it occupies lesser area and are produced on silicon sibstrate unlike resistors.

4. For depletion mode transistor, gate should be connected to
a) source
b) drain
c) ground
d) positive voltage rail

Answer: a
Explanation: For the depletion mode transistor, gate is connected to source so it is always on and only the characteristic curve Vgs=0 is relevant.

5. In nMOS inverter configuration depletion mode device is called as
a) pull up
b) pull down
c) all of the mentioned

d) none of the mentioned

Answer: a
Explanation: In nMOS inverter configuration, depletion mode devices are called as pull up and enhancement mode devices are called as pull down transistor.

7. The ratio of Zp.u/Zp.d is given by
a) 1/4
b) 4/1
c) 1/2
d) 2/1

Answer: b
Explanation: The ratio of Zp.u/Zp.d where Z is determined by the length to width ratio of the transistor, is given by 4/1.

8. Pass transistors are transistors used as
a) switches connected in series
b) switches connected in parallel
c) inverters used in series
d) inverter used in parallel

Answer: a
Explanation: Pass transistors are transistor used as switches in series with lines carrying logic levels due to its isolated nature of the gate.

9. An inverter driven through one or more pass transistors has Zp.u/Zp.d ratio of
a) 1/4
b) 4/1
c) 1/8
d) 8/1

Answer: d
Explanation: An inverter driven directly from output of another has the ratio of 4/1 and if driven through one or more pass transistors has the ratio of 8/1.

10. In depletion mode pull-up, dissipation is high since current flows when
a) Vin = 1
b) Vin = 0
c) Vout = 1
d) Vout = 0

Answer: a
Explanation: In nMOS depletion mode pull-up, dissipation is high since current flows Vin = logical 1.

11. In complementary transistor pull-up, current flows when
a) Vin = 1
b) Vin = 0
c) current doesn't flow
d) Vout = Vin

Answer: c
Explanation: In complementary transistor pull-up no current flows either for logical 1 or 0, full logical 1 and 0 levels are presented at the output.

CMOS Inverter

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "CMOS Inverter".

1. CMOS inverter has_____regions of operation
a) three
b) four
c) two
d) five

Answer: d
Explanation: CMOS inverter has five distint regions of operation which can be determined by plotting CMOS inverter current versus Vin.

2. If n-transistor conducts and has large voltage between source and drain, then it is said to be in _____region
a) linear
b) saturation
c) non saturation
d) cut-off

Answer: b
Explanation: If n-transistor conducts and has large voltage between source and drain, then it is in saturation.

3. If p-transistor is conducting and has small voltage between source and drain, then the it is said to work in
a) linear region
b) saturation region
c) non saturation resistive region
d) cut-off region

Answer: c
Explanation: If p-transistor is conducting and has small voltage between source and drain, then it is said to be in unsaturated resistive region.

4. In the region where inverter exhibits gain, the two transistors are in __ _____region
a) linear
b) cut-off
c) non saturation
d) saturation

Answer: d
Explanation: In the region where the inverter exhibits gain, the two transistors n and p operates in saturation region.

5. If both the transistors are in saturation, then they act as
a) current source
b) voltage source
c) divider
d) buffer

Answer: a
Explanation: When both the transistors are in saturation, then act as current sources so that the equivalent circuit is two current sources between Vdd and Vss.

6. If $\beta n = \beta p$, then Vin is equal to
a) Vdd
b) Vss
c) 2Vdd
d) 0.5Vdd

Answer: d
Explanation: If $\beta n = \beta p$, then Vin = 0.5Vdd which implies that the changeover between logic levels is symmetrically disposed about the point.

7. Mobility depends on
a) transverse electric field
b) Vg
c) Vdd
d) Channel length

Answer: a
Explanation: Mobility is affected by transverse electric field and thus also depends on Vgs and the mobility of p-device and n-device are inherently unequal.

8. In CMOS inverter, transistor is a switch having
a) infinite on resistance
b) finite off resistance
c) buffer
d) infinite off resistance

Answer: b
Explanation: In CMOS inverter, transistor is a awitch having finite on resistance and infinite off resistance.

9. CMOS inverter has_____output impedance
a) low
b) high

Answer: a
Explanation: CMOS inverter has low output impedance and this makes it less prone to noise and disturbance.

10. Input resistance of CMOS inverter is
a) high
b) low

Answer: a
Explanation: Input resistance of CMOS inverter is extremely high as it is a perfect insulator and draws no dc input source.

11. Increasing fan-out,_____the propogation delay
a) increases
b) decreases
c) does not affect

d) exponentially decreases

Answer: a
Explanation: In CMOS inverter, increasing the fan-out also increases the propogation delay. Fan-out is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed.

12. Fast gate can be built by keeping
a) low output capacitance
b) high on resistance
c) high output capacitance
d) input capacitance does not affect speed of the gate

Answer: a
Explanation: Fast gate can be built by keeping the output capacitance small and by decreasing the on resistance of the transistor.

Characteristics of npn Bipolar Transistors

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "Characteristics of npn Bipolar Transistors".

1. Transconductance of a bipolar is given by
a) (kT/q)/Ic
b) Ic/(kT/q)
c) (q/KT)/Ic
d) Ic/(q/KT)

Answer: b
Explanation: Transconductance gm of a bipolar transistor is given by gm = Ic/(kT/q). Transconductance is the electrical characteristic relating the current through the output of a device to the voltage across the input of a device.

2. Transconductance depends on the process.
a) true
b) false

Answer: b
Explanation: Transconductance gm is independent of process.

3. gm is_____on input voltage Vbe
a) inversely proportional
b) proportional
c) exponentially dependent
d) is not dependent

Answer: c
Explanation: Transconductance gm is exponentially dependent on input voltage Vbe (base to emitter voltage).

4. gm is_____to Ic
a) directly proportional
b) inversely proportional
c) not dependent
d) exponentially proportional

Answer: a
Explanation: Transconductance gm is directly proportional to Ic, collector current.

5. Transconductance is a
a) weak function
b) strong function
c) both
d) none of the mentioned

6. gm of bipolar is less than gm of MOS.
a) true
b) false

Answer: b
Explanation: Transconductance gm of bipolar is greater than gm of MOS if inputs are controlled by equal amounts of charge.

7. Which of the following is true when inputs are controlled by equal amounts of charge?
a) Cg(MOS) = Cbase(bipolar)
b) Cg(MOS) greater than Cbase(bipolar)
c) Cg(MOS) lesser than Cbase(bipolar)
d) Cs(MOS) lesser than Cbase(bipolar)

Answer: a
Explanation: Cg(MOS) = Cbase(bipolar) when inputs are controlled by equal amounts of charge, and then gm(bipolar) >> gm(MOS).

8. Which has better I/A ?
a) CMOS
b) bipolar
c) nMOS
d) pMOS

Answer: b
Explanation: Current/Area (I/A) of bipolar is five times better than CMOS and this can be calculated using base resistance and base transit time.

9. Bipolar transistor exhibits_____delay
a) turn on
b) turn off
c) storage
d) all of the mentioned

Answer: d
Explanation: Bipolar transistors exhibits tun-on, turn-off, storage delays.

10. In bipolar transistor, which is heavily doped?
a) base region
b) emitter region
c) collector region
d) base and emitter

Answer: b
Explanation: In bipolar transistor, emitter region is heavily doped and base region is lightly doped.

11. Bipolar transistor is a symmetrical device.
a) true
b) false

Answer: b
Explanation: Bipolar transistor is not symmetrical like other transistors.

BiCMOS Inverters

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “BiCMOS Inverters”.

1. In BiCMOS, bipolar transistors are used to
a) drive input loads
b) drive output loads
c) to perform logic functions
d) to amplify the input voltage

Answer: b
Explanation: In BiCMOS, bipolar transistors are used to drive output loads. Bipolar transistor can also be used as amplifier, switch or as an oscillator.

2. In BiCMOS, MOS switches are used to
a) drive input loads
b) drive output loads
c) to perform logic functions
d) to amplify the input voltage

Answer: c
Explanation: In BiCMOS circuits, MOS switches are used to perform logic functions. The ability to turn the power MOS “ON” and “OFF” allows the device to be used as a very efficient switch with switching speeds much faster than standard bipolar junction transistors.

3. The nMOS and pMOS transistors used in BiCMOS is
a) depletion mode
b) enhancement mode
c) only pMOS
d) only nMOS

Answer: b
Explanation: The nMOS and pMOS transistors used in BiCMOS device operates in enhancement mode. Enhancement mode devices are mostly common switching elements in MOS.

4. The inverter has
a) low input impedance
b) high input impedance
c) high output impedance
d) high input and output impedance

Answer: a
Explanation: The inverter has low input impedance. The basic inverter circuit requires a transistor with source connected to ground and a load resistor connected from the drain to positie supply Vdd.

5. The inverter has
a) low output impedance
b) low input impedance
c) low power dissipation
d) high input and output impedance

Answer: a
Explanation: The inverter has low output impedance and low input impedance. These are some of the properties of a BiCMOS inverter.

6. The inverter has
a) high current driving capability
b) occupies smaller area
c) high noise margin
d) all of the mentioned

Answer: d
Explanation: The inverter has high current driving capability, occupies smaller area and has high noise margins.

7. Output voltage swing should be reduced for a better performance of BiCMOS circuit.
a) true
b) false

8. BiCMOS inverter requires high load current sourcing.
a) true
b) false

Answer: a
Explanation: BiCMOS inverter needs high load current sinking and sourcing. Sinking provides a grounded connection to the load, whereas sourcing provides a voltage source to the load.

9. BiCMOS has_____standby leakage current
a) higher
b) lower

Answer: a
Explanation: BiCMOS has higher standby leakage current and thus has high power consumption.

10. For improved base current discharge,_____ enhancement type nMOS devices have to be added
a) two
b) three
c) one
d) four

Answer: a
Explanation: For improved base current discharge, two enhancement type nMOS transistors have to be added.

11. The BJTs in the BICMOS circuit is in_____configuration:
a) Push-pull
b) Totem pole
c) Active high
d) Active low

Answer: b
Explanation: In BiCMOS circuit, the BJT transistors are in Totem pole configuration.

12. The MOSFETS are arranged in this configuration to provide:
a) Zero static power dissipation
b) High Input impedance
c) Both zero static power dissipation and high input imedance
d) None of the mentioned

Answer: c
Explanation: MOSFETs provide zero static power dissipation and high input impedance.

Latch-up in CMOS

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Latch-up in CMOS”.

1. In latch-up condition, parasitic component gives rise to_____conducting path
a) low resistance
b) high resistance
c) low capacitance
d) high capacitance

Answer: a
Explanation: In latch-up condition, parasitic component gives rise to low resistance conducting path between Vdd and Vss with disastrous results. Carefull control during fabrication is necessary to avoid this problem.

2. Latch-up can be induced by
a) incident radiation
b) reflected radiation
c) etching
d) diffracted radiation

Answer: a
Explanation: Latch-up can be induced by glitches on the supply rail or by incident radiation.

3. How many transistors might bring up latch up effect in p-well structure?
a) two
b) three
c) one
d) four

Answer: a
Explanation: Two transistors and two resistances might bring up the latch-up effect in p-well structure. These are associated with p-well and with regions of the substrate.

4. Substrate doping level should be decreased to avoid the latch-up effect.
a) true
b) false

Answer: b
Explanation: An increase in substrate doping level with a consequent drop in the value of Rs can be used as a remedy for latch-up problem.

5. What can be introduced to reduce the latch-up effect?
a) latch-up rings
b) guard rings
c) latch guard rings

d) substrate rings

Answer: b
Explanation: The introduction of guard rings can reduce the effect of latch-up problem. Guard rings are diffusions which decouple the parasitic bipolar transistors.

6. Which process produces circuit which are less prone to latch-up effect?
a) CMOS
b) nMOS
c) pMOS
d) BiCMOS

Answer: d
Explanation: BiCMOS process produces circuits which are less likely to suffer from latch-up problems where as CMOS circuits are very highly prone to latch-up problems.

7. One of the factor in reducing the latch-up effect is
a) reduced p-well resistance
b) reduced n-well resistance
c) increased n-well resistance
d) increased p-well resistance

Answer: b
Explanation: One of the main factor in reducing the latch-up effect is reduced n-well resistance Rw. Reduction in Rw means that a larger lateral current is necessary to invite latch-up and higher value of holding current is also required.

8. The parasitic pnp transistor has the effect of_____carrier lifetime
a) increasing
b) decreasing
c) exponentially decreasing
d) exponentially increasing

Answer: b
Explanation: The parasitic pnp transistor has the effect of reducing carrier lifetime in the n-base region.

9. The reduction in carrier lifetime brings about
a) reduction in alpha
b) reduction in beta
c) reduction in current

d) reduction in voltage

Answer: b
Explanation: The parasitic pnp transistor has the effect of reducing carrier lifetime in the n-base region which results in radiation in beta.

10. To reduce latch-up effect substrate resistance should be high.
a) true
b) false

Answer: b
Explanation: To reduce the latch-up effect, substrate resistance Rs should be low. Reduction of Rs and Rw means that larger lateral current is necessary to invite latch-up.

11. Latch-up is the generation of
a) low impedance path
b) high impedance path
c) low resistance path
d) high resistance path

Answer: a
Explanation: Latch-up is the generation of low-impedance path in CMOS chips between the power suppply and ground rails.

12. Latch-up is brought about by BJTs
a) with positive feedback
b) with negative feedback
c) with no feedback
d) without BJT

Answer: a
Explanation: Latch-up occurs due to BJTs for a silicon-controlled rectifiers with positive feedback and virtually short circuit the power and ground rail.

13. Sudden transient in power can cause latch-up.
a) true
b) false

Answer: a
Explanation: Sudden transient in power and ground buses are also among the reason which causes latch-up effect.

14. BJT gain should be_____to avoid latch-up effect
a) increased
b) decreased
c) should be maintained constant
d) changed randomly

Answer: b
Explanation: BJT gain should be reduced by lowering the minority carrier lifetime through doping of the substrate to lower the latch-up effect.

BiCMOS Logic Gates

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "BiCMOS Logic Gates".

1. The BiCMOS are preferred over CMOS due to:
a) Switching speed is more compared to CMOS
b) Sensitivity is less with respect to load capacitance
c) High current drive capability
d) All of the mentioned

Answer: d
Explanation: These are the 3 advantages of BiCMOS over CMOS.

2. The transistors used in BiCMOS are:
a) BJT
b) MOSFET
c) Both BJT and MOSFETs
d) JFET

Answer: c
Explanation: BiCMOS is a combination of both MOSFET and BJT.

3. The high current driving capability of the BiCMOS is due to:
a) NMOS in saturation mode
b) PMOS in saturation mode
c) CMOS

d) BJT

Answer: d
Explanation: BJT has the high current driving capability.

4. In BiCMOS inverter, the BJT used are:
a) Only Npn BJT
b) Only Pnp BJT
c) Both npn and pnp BJT
d) Multi emitter npn BJT

Answer: a
Explanation: npn BJTs are used in BiCMOS inverter.

5. The drawback of the BiCMOS circuits are:
a) Sensitivity is less load capacitance
b) Bipolar transistors are used for driving current to the load capacitance but not for the logic operations
c) Increased fabrication Complexity
d) All of the mentioned

Answer: c
Explanation: The other 2 are the merits of BiCMOS, Increased fabrication Complexity is a demerit of BiCMOS circuits.

6. The Bipolar Transistor is fabricated on :
a) Same substrate of nMOS
b) N-well in p Substrate
c) P-well in n Substrate
d) Same substrate of pMOS

Answer: a
Explanation: BiCMOS is fabricated on the same substrate of nMOS.

7. The n-well created for Bipolar Transistor in BiCMOS is used as:
a) Substrate
b) Collector
c) Emitter
d) None of the mentioned

Answer: b
Explanation: The created nWell is used as Collector region for BiCMOS.

8. The n-well collector is formed by:
a) Lightly doped n-type epitaxial layer on p-Substrate
b) Heavily doped n-type epitaxial layer on p-Substrate
c) Lightly doped n-type diffused layer on p-Substrate
d) Heavily doped n-type diffused layer on p-Substrate

Answer: a
Explanation: To make the doping concentration less than the emitter.

9. The collector contact region is doped with higher concentration of n-type impurities due to:
a) It creates a depletion region at the contact surface
b) It creates a low conductivity path between collector region and contact
c) It reduces a contact resistance
d) It can withstand high voltages as compared to collector region

Answer: c
Explanation: The collector contact region is doped with higher concentration of n-type impurities reduces contact resistance.

Stick Diagram

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Stick Diagram”.

1. Stick diagrams are those which convey layer information through
a) thickness
b) color
c) shapes
d) layers

Answer: b
Explanation: Stick diagrams are those which convey layer information through color codes. Thickness is not considered in this stick diagram representation.

2. Which color is used for n-diffusion?
a) red
b) blue
c) green

d) yellow

Answer: c
Explanation: Green color is used to show the presence of n-diffusion layer. The n-type diffusion will dope the source or drain region in the p-well region.

3. Which color is used for implant?
a) red
b) blue
c) green
d) yellow

Answer: d
Explanation: Yellow color is used to represent implant layer.

4. Which color is used for contact areas?
a) red
b) brown
c) black
d) blue

Answer: c
Explanation: Black color is used to represent contact areas. This is the part where two different touch or cross each other.

5. Which color is used for polysilicon?
a) brown
b) red
c) white
d) orange

Answer: b
Explanation: Red is used to represent polysilicon layers. It is a semi-conductor like material and is a hyper pure form of silicon.

6. Which color is used for polysilicon 2?
a) blue
b) brown
c) orange
d) white

Answer: c
Explanation: Orange color is used to represent polysilicon-2 layer.

7. Which color is used for buried contact?
a) black
b) white
c) green
d) brown

Answer: d
Explanation: Brown color is used to represent buried contact. Buried contact is most widely used, subject to fewer design rule restrictions and are smaller in area.

8. n and p transistors are separated by using
a) differentiation line
b) separation line
c) demarcation line
d) black line

Answer: c
Explanation: Demarcation line separates n and p transistors. Demarcation line is similar to dotted line in brown.

9. _____layer should be over_____layer
a) ntype, polysilicon
b) polysilicon, ntype

Answer: b
Explanation: Polysilicon layer should be over n-type layer. This is the standard pattern used in stick diagram representation.

11. Implant is represented using
a) black, dark line
b) black, dotted line
c) yellow, dark line
d) yellow, dotted line

Answer: d
Explanation: Implant is represented using yellow color dotted lines. It is drawn in the middle of the nMOS or pMOS whereever the implant is used.

12. Stick diagram gives the position of placement of the element.
a) true
b) false

Answer: b
Explanation: Stick diagram does not show exact placement of components, transistor length, wire length and width, tub boundaries etc.

13. When two or more cuts of same type cross or touch each other, that represents
a) contact cut
b) electrical contact
c) like contact
d) cross contact

Answer: b
Explanation: When two or more sticks of same type cross or touch each other, then that forms a contact called electrical contact.

Design Rules and Layout-1

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "Design Rules and Layout-1".

1. Circuit design concepts can also be represented using symbolic diagram.
a) true
b) false

Answer: a
Explanation: Circuit design concepts can be represented using stick diagrams and symbolic diagrams. Stick diagrams represents different layers with color codes. Symbolic diagram represents the structure with symbols with color codes.

2. Circuit designers need_____circuits
a) tighter
b) smaller layout
c) decreased silicon area
d) all of the mentioned

Answer: d
Explanation: Circuit designers in general prefer tighter, smaller layouts for improved performance and decreased silicon area.

3. Process engineers want_____process
a) smaller
b) tighter
c) reproducible
d) non reproducible

Answer: c
Explanation: Process engineers wants design rules which are controllable and reproducible process.

4. Maturity level of the process line affects design rules.
a) true
b) false

Answer: a
Explanation: Yes, the maturity level of the process line affects design rules.

5. Design rules does not specify
a) linewidths
b) separations
c) extensions
d) colours

Answer: d
Explanation: Design rules specify line widths, separations and extensions in terms of lambda.

6. The width of n-diffusion and p-diffusion layer should be
a) 3λ
b) 2λ
c) λ
d) 4λ
Answer: b
Explanation: The width of n-diffusion and p-diffusion should be 2λ according to design rules.

7. What should be the spacing between two diffusion layers?
a) 4λ
b) λ
c) 3λ

d) 2λ

Answer: c
Explanation: The spacing between two diffusion layers should be 3λ according to design rules and standards.

8. What should be the width of metal 1 and metal 2 layers?
a) 3λ, 3λ
b) 2λ, 3λ
c) 3λ, 4λ
d) 4λ, 3λ

Answer: c
Explanation: The width of the metal 1 layer should be 3λ and metal 2 should be 4λ.

9. Implant should extend_____from all the channels
a) 2λ
b) 3λ
c) 4λ
d) λ

Answer: a
Explanation: Implant for a n-mos depletion mode transistor should extend minimum of 2λ from the channel in all the directions.

10. Which type of contact cuts are better?
a) buried contacts
b) butted contacts
c) butted & buried contacts
d) none of the mentioned

Answer: a
Explanation: Buried contacts are much better than butted contacts. In butted contacts the two layers are joined together or binded together using adhesive type of material where as in buried contact one layer is interconcted or fitted into another.

11. Which design method occupies or uses lesser area?
a) lambda rules
b) micron rules
c) layer rule

d) source rule

Answer: b
Explanation: Micron rules occupies or consumes lesser area. 50% of the area usage can be reduced by using micron rules over lambda rules.

12. Which gives scalable design rules?
a) lambda rules
b) micron rules
c) layer rules
d) thickness rules

Answer: a
Explanation: Lambda rules gives scalable design rules and micron rules gives absolute dimensions.

13. Devices designed with lambda design rules are prone to shorts and opens.
a) true
b) false

Answers: b
Explanation: Lambda design rules prevents shorting, opens, contact from slipping out of area to be contacted.

Design Rules and Layout-2

This set of VLSI Questions and Answers for Freshers focuses on “Design Rules and Layout-2”.

1. Diffusion and polysilicon layers are connected together using
a) butting contact
b) buried contact
c) separate contact
d) cannot be connected

Answer: a
Explanation: Diffusion and polysilicon layer are joined together using butting contact. In butting contact the two layers are joined or binded together.

2. Which is more complex process?
a) buried contact

b) butting contact
c) buried & butting contact
d) none of the mentioned

Answer: a
Explanation: Butting contact is complex process whereas buried contact is simple process because butting contact should be done more carefully to serve well and be strong.

3. Which contact cut occupies smaller area?
a) buried contact
b) butting contact
c) buried & butting contact
d) none of the mentioned

Answer: a
Explanation: Buried contact occupies smaller area than butting contact as in buried contacts one layer will be completely within or almost within the another layer.

4. Isolation layer between two metal layers must be thinner.
a) true
b) false
Answer: b
Explanation: Isolation layer between two metal layers should be thicker. Metal to metal separation is large and is brought about mainly by difficulties in defining metal edges accurately.

5. The oxide layer below the first metal layer is deposited using
a) diffusion method
b) chemical vapour deposition
c) solid deposition
d) scattering method

Answer: b
Explanation: The oxide layer below the first metal layer is depostied using chemical vapour deposition method. This is a chemical process used to produce high quality high performance solid materials.

6. Which layer is used for power and signal lines?
a) metal
b) polysiicon
c) n-diffusion
d) p-diffusion

Answer: a
Explanation: Metal layers are used for power and signal lines as metals has good thermal and electrical conductivity.

7. Minimum feature size for thick oxide is
a) 2λ
b) 3λ
c) 4λ
d) λ

Answer: b
Explanation: The minimum feature size for thick oxide is 3λ and minimum separation between thinox regions is also 3λ.

8. Hatching is compatible with
a) monochrome encoding
b) bicode encoding
c) tricode encoding
d) not compatible with any encoding

Answer: a
Explanation: Hatching is compatible with monochrome encoding and also may be added to color mask coding. It is designed using closely spaced lines or sticks.

9. Minimum n-well width should be_____micro meter
a) 2
b) 3
c) 4
d) 6
Answer: b
Explanation: The minimum width of n-well is 3 micro meter because n-well should be with little thickness and in it p-type devices are formed.

10. The minimum spacing between two n-well is_____micro meter
a) 4
b) 5
c) 8
d) 8.5

Answer: d
Explanation: The minimum spacing between two n-well is 8.5 micro meter according to the lambda based design rules.

11. Which can bring about variations in threshold voltage?
a) oxide thickness
b) ion implantation
c) poly variations
d) all of the mentioned

Answer: d
Explanation: One of the problem in the manufacture using design rule is that variation in threshold voltage occurs. And this is caused by oxide thickness, ion implantation and poly variations.

12. Advantages of design rules are
a) durable
b) scalable
c) portable
d) all of the mentioned

Answer: d
Explanation: Some of the advantages of generalised design rules are those are durable, scalable, portable, increases designer efficiency and automatic translation to final layout can be done.

13. Minimum diffusion space is
a) 2λ
b) 3λ
c) 4λ
d) λ

Answer: b
Explanation: Minimum diffusion space is 3λ to avoid the possibility of their associated regions overlapping and conducting current.

14. Contact cuts should be_____apart
a) 2λ
b) 3λ
c) 4λ
d) λ

Answer: a
Explanation: Two contact cuts should be 2λ apart to prevent holes from merging.

Sheet Resistance

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Sheet Resistance”.

1. Area A of a slab can be given as
a) t * W
b) t / W
c) L * W
d) L * t

Answer: a
Explanation: Area A of a uniform slab is given as the product of thickness t and width W of the slab. Its unit is $(\text{micrometer})^2$.

2. For 5 micron technology, the Rs value for a metal is
a) 0.03
b) 0.04
c) 0.02
d) 0.01

Answer: a
Explanation: For a 5 micron technology, the Rs value for a metal is 0.03. It is the standard typical sheet resistance values.

3. For 2 micron technology, the Rs value for polysilicon is
a) 10-40
b) 20-50
c) 15-30
d) 15-100

Answer: c
Explanation: For 2 micron technology, the Rs value for polysilicon is 15-30.

4. Which has higher Rs values?
a) n-diffusion
b) p-diffusion
c) both of the mentioned
d) none of the mentioned

Answer: b
Explanation: The Rs values for p-diffusion is 2.5 times greater than that of the n-diffusion.

5. For 1.2 micron technology, the Rs value for diffusion is
a) 20-40
b) 20-45
c) 15-30
d) 25-50

Answer: b
Explanation: For 1.2 micron technology, the Rs value for diffusion is 20-45.

6. What is the relationship between channel resistance and sheet resistance?
a) R = Rs
b) R = Z*Rs
c) R = Z/Rs
d) R = Rs/Z

Answer: b
Explanation: The relationship between channel resistance and sheet resistance can be given as R = Z*Rs. Sheet resistance is a measure of resistance of thin films that are nominally uniform in thickness.

7. Z can be given as the ration of
a) lower channel by upper channel
b) upper channel by lower channel
c) all of the mentioned
d) none of the mentioned

Answer: b
Explanation: Z (length to width) ratio can be given as the ratio of upper channel to lower channel. It is just a numerical quantity and has no unit.

8. Deposition of metal or silicon alloy can be done by
a) sputtering
b) evaporation
c) sputtering and evaporation
d) deposition should not be made

Answer: c
Explanation: Deposition of metal or silicon alloy can be done by either sputtering or evaporation. Sputtering is a process whereby particles are ejected from a solid target material due to bombardment of the target by energetic particles.

9. Deposition of metal can be done by co-evaporation.
a) true
b) false

Answer: a
Explanation: Deposition of metal or silicon alloy can also be done by co-evaporation from the elements.

10. Processing of the device is better using
a) polysilicon
b) silicides
c) both of the mentioned
d) none of the mentioned

Answer: a
Explanation: Processing of the device is better using polysilicon than silicides even though the properties of silicides are better than polysilicon.

Area Capacitance

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "Area Capacitance".

1. Conducting layer is separated from substrate using
a) dielectric layer
b) silicon layer
c) metal layer
d) diffusion layer

Answer: a
Explanation: Conducting layer is separated from the substrate by using dielectric or insulating layer as both are electrical insulators that can be polarized by an applied electric field.

2. Gate to channel capacitance of 5 micron technology is_____pF X $10^{(-4)}$ $(micrometer)^2$.
a) 1
b) 2
c) 4
d) 0.4

Answer: c
Explanation: Gate to channel capacitance of 5 micron technology is 4 pF X $10^{(-4)}$ $(\text{micrometer})^2$. It is the standard typical calculated value.

3. Area capacitance of diffusion region of 2 micron technology is_____pF X $10^{(-4)}$ $(\text{micrometer})^2$.
a) 2
b) 2.75
c) 3.75
d) 4.75

Answer: c
Explanation: Area capacitane of diffusion region of 2 micron technology is 3.75 pF X $10^{(-4)}$ $(\text{micrometer})^2$.

4. Relative capacitance of diffusion region of 5 micron technology is
a) 1
b) 0.25
c) 1.25
d) 2

Answer: b
Explanation: The relative capacitance of diffusion region of 5 micron technology is 0.25. The relative value is calculated by comparing two values of same type.

5. A feature size square has
a) L > W
b) W > L
c) L = W
d) L > d

Answer: c
Explanation: A feature size square has L = W and its gate to channel capacitance value is called as square Cg.

6. The standard square Cg value of a 5 micron technology is
a) 0.01 pF
b) 0.1 pF
c) 1 pF
d) 10 pF

Answer: a
Explanation: The standard square Cg value of a 5 micron technology is 0.01 pF. This standard square Cg value can be calculated by using the area of standard square value and the capacitance value.

7. The standard square Cg value of a 1.2 micron technology is
a) 0.01 pF
b) 0.0023 pF
c) 0.023 pF
d) 0.23 pF

Answer: b
Explanation: The standard square Cg value of a 1.2 micron technology is 0.0023 pF.

8. Relative area for L = 20λ and W = 3λ is
a) 10
b) 15
c) 1/15
d) 1/10

Answer: b
Explanation: Relative area for L = 20λ and W = 3λ is = (20λ X 3λ) / (2λ X 2λ) = 15. Relative area has no unit as two quantities of same type have been used.

9. The value of gate capacitance is
a) 0.25 square Cg
b) 1 square Cg
c) 1.25 square Cg
d) 1.5 square Cg

Answer: b
Explanation: The value of gate capacitance is one square Cg. This is the standard value.

10. Delay unit of 5 micron technology is
a) 1 nsec
b) 0.1 nsec
c) 0.01 nsec
d) 1 sec

Answer: b
Explanation: Delay unit of 5 micron technology is 0.1 nsec.

11. Delay unit of 1.2 micron technology is
a) 0.064 nsec
b) 0.0064 nsec
c) 0.046 nsec
d) 0.0046 nsec

Answer: c
Explanation: The delay unit of 1.2 micron technology is 0.046 nsec.

12. What is the transition point of an inverter?
a) Vdd
b) 0.5 Vdd
c) 0.25 Vdd
d) 2 Vdd

Answer: b
Explanation: The transition point of an inverter is 0.5 Vdd. Transition point is the point where different phases of same substance can be obtained in equilibrium.

13. What is the desired or safe delay value for 5 micron technology?
a) 0.3 nsec
b) 0.5 nsec
c) 0.1 nsec
d) 0.2 nsec

Answer: a
Explanation: The desired or safe delay value for 5 micron technology is 0.3 nsec.

Inverter Delays

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Inverter Delays”.

1. The resistance value associated with Rp.u is
a) 2Rs
b) Rs
c) 4Rs
d) Rs/2

Answer: c
Explanation: The resistance value associated with Rp.u. is 4Rs. Resistance is the measure of difficulty to pass an electric current through that material.

2. The resistance value associated with Rp.d. is
a) 2Rs
b) Rs
c) 4Rs
d) Rs/2

Answer: b
Explanation: The resistance value associated with Rp.d. is 1Rs. This is the measure of difficulty to pass current through the pull-down device.

3. The overall delay of nMOS inverter pair is
a) 4Ƭ
b) Ƭ
c) 5Ƭ
d) 2Ƭ

Answer: c
Explanation: The overall delay of nMOS inverter pair is Ƭ +4Ƭ = 5Ƭ . This delay is the time taken for the input signal to get inverted and arrive at the output.

4. The inverter pair delay for inverters having 4:1 ratio is
a) 4Ƭ
b) Ƭ
c) 5Ƭ
d) 2Ƭ

Answer: c
Explanation: The inverter pair delay for inverters having 4:1 ratio is 5Ƭ . This measure of delay is for two inverters, in which the output of the first is given as the input for the second inverter.

5. The assymetry of resistance value can be eliminated by
a) decreasing the width
b) increasing the width
c) increasing the length
d) increasing the width

Answer: b
Explanation: The assymetry of resistance value can be eliminated by increasing the width of the p-device channel.

6. The ratio of rise time to fall time can be equated to
a) βn/βp
b) βp/βn
c) βp*βn
d) βp/2βn

Answer: a
Explanation: The ratio of rise time to fall time can be equated to βn/βp. Rise time is the time taken by a signal to change from a specified low value to a specified high value. Fall time is the time taken for the amplitude of a pulse to decrease from a specified value to another specified value.

7. The value μn is equal to
a) μp
b) 0.5μp
c) 1.5μp
d) 2.5μp

Answer: d
Explanation: The value of μn = 2.5 μp. This shows that μn value is greater than that of the μp.

8. Which quantity is slower?
a) rise time
b) fall time
c) all of the mentioned
d) none of the mentioned

Answer: a
Explanation: Rise time is slower by a factor of 2.5 than fall time.

9. Condition for achieving symmetrical operation is
a) Wp = Wn
b) Wp greater than Wn
c) Wp lesser than Wn
d) Wp lesser than 2Wn

Answer: b
Explanation: The condition for achieving symmetrical operation is Wp = 2.5 Wn.

10. Rise time and fall time is_____to load capacitance CL
a) directly proportional
b) inversely proportonal
c) exponentially equal
d) not related

Answer: a
Explanation: Rise time and fall time is directly proportional to load capacitance CL.

11. Rise time and fall time is_____to Vdd
a) directly proportional
b) inversely proportonal
c) exponentially equal
d) not related

Answer: b
Explanation: Rise time and fall time is inversely proportional to Vdd. This shows that if Vdd is reduced fall time and rise time increases.

VLSI Questions and Answers – Drivers

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "Drivers".

1. For shorter delays_____resistance should be used
a) smaller
b) larger
c) does not depend on resistance
d) very large

Answer: a
Explanation: For shorter delays low resistance should be used as delay is directly proportional or related to resistance.

2. To reduce resistance value of inverters, channels must be made
a) wider
b) narrower
c) lenghthier
d) shorter

Answer: a
Explanation: Channels must be made wider to reduce the resistance value that is low resistance values for Zp.u. ad Zp.d. imply low L:W ratios and thus consequently an inverter to meet this need occupies a larger area.

3. As width increases, capacitive load
a) increases
b) decreases
c) does not change
d) exponentially increases

Answer: a
Explanation: As width of the channel increases, capacitive load also increases and with this the area occupied also increases. The rate at which the width increases affects the stages N and load capacitance.

4. Delay per stage for logic 0 to 1 transition can be given as
a) fτ
b) 2fτ
c) 3fτ
d) 4fτ

Answer: a
Explanation: Delay per stage for logic 0 to 1 transition can be given as fτ . With large f, N decreases but delay per stage increases.

5. Delay per stage for logic 1 to 0 transition can be given as
a) fτ
b) 2fτ
c) 3fτ
d) 4fτ

Answer: d
Explanation: Delay per stage for logic 1 to 0 transition can be given as 4fτ . Using the delay for transition from 1 to 0 and 0 to 1 total nMOS delay can be obtained.

6. Total delay of an nMOS pair is
a) fτ
b) 2fτ
c) 5fτ
d) 4fτ

Answer: c
Explanation: Total delay of an nMOS pair is equal to 5fτ . This can be calculated by knowing delay per stage, that is for two different transitions from 0 to 1 and vice versa.

7. Total delay of an CMOS pair is
a) 5fτ
b) 7fτ
c) 8fτ
d) 4fτ

Answer: b
Explanation: Total delay of an CMOS pair is equal to 7fτ . This can be calculated by knowing thee delay per stage of CMOS.

8. The number of stages N can be given as
a) ln(y)*ln(f)
b) ln(y)/ln(f)
c) ln(f)/ln(y)
d) ln(f)/ln(2y)

Answer: b
Explanation: The number of stages N can be given as ln(y)/ln(f). By knowing whether the number of stages N is even or odd we can calculate the total delay for nMOS, CMOS etc.

9. When number of stages N is even, the total delay for nMOS can be given as
a) 1.5Nfτ
b) 2.5Nfτ
c) 3.5Nfτ
d) 4.5Nfτ

Answer: b
Explanation: When number of stages N is even, the total delay for nMOS can be given as 2.5Nfτ . This is calculated by using the formula (N/2)*5fτ .

10. When number of stages N is even, the total delay for CMOS can be given as
a) 1.5Nfτ
b) 2.5Nfτ
c) 3.5Nfτ
d) 4.5Nfτ

Answer: c
Explanation: When number of stages N is even, the total delay for CMOS can be given as 3.5Nf$_T$. This is calculated by using the formula (N/2)*7f$_T$.

11. In BiCMOS drivers, the input voltage Vbe is _____on base width
a) directly proportional
b) inversely proportional
c) logarithmically proportional
d) exponentially proportional

Answer: c
Explanation: In BiCMOS driver, the input voltage Vbe is logarithmically proportional to the base width Wb and on electron mobility.

12. Which has larger value?
a) Tin
b) TL
c) Rc
d) None of the mentioned

Answer: a
Explanation: In BiCMOS drivers, the initial time Tin necessary to charge base emitter junction is larger than the time TL requires to charge the output load capacitance.

13. In BiCMOS driver, a good bipolar transistor should have
a) low Rc
b) high hfe
c) high gm
d) all of the mentioned

Answer: d
Explanation: In BiCMOS drivers, a good bipolar transistor should have low Rc, high hfe, high gm etc.

Propogation Delays

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Propogation Delays”.

1. Propogation time is directly proportional to
a) x
b) 1/x
c) x^2
d) $1/x^2$

Answer: c
Explanation: Propogation time is directly proportional to square of the propogation distance (x^2). It is the time taken by the signal to move from input port to output port.

2. The total resistance can be given as
a) nRs
b) nrRs
c) rRs
d) Rs

Answer: b
Explanation: The total resistance can be given as the product of nrRs where r is the relative resistance per section in terms of Rs.

3. Total capacitance can be given as
a) n(square Cg)
b) nc(square Cg)
c) c(square Cg)
d) square Cg

Answer: b
Explanation: Total capacitance can be given as the product of nc(square Cg) where c is the relative capacitance per section in terms of square Cg.

4. Overall delay is directly proportional to
a) n
b) 1/n
c) n^2
d) $1/n^2$

Answer: c
Explanation: The overall delay is directly proportional to n^2, where n is the number of pass transistors in series.

5. The number of pass transistors connected in series can be increased if
a) compressor is connected

b) buffer is connected
c) ground is connected
d) voltage regulator is connected

Answer: b
Explanation: The number of pass transistors connected in series can be increased by connecting buffer in between.

6. Buffer is used because
a) it increases the speed
b) decreases senstivity to noise
c) decreases speed
d) does not affect speed

Answer: a
Explanation: Buffer is used for long polysilicon runs because it increses the speed and reduces the sensitivity to noise.

7. The overall delay is_____to the relative resistance r
a) directly proportional
b) inversely proportional
c) exponentially proportional
d) not dependent

Answer: a
Explanation: The overall delay is directly proportional to the relative resistance r. Overall delay is given as product of n^2rcτ .

8. Small disturbances of noise
a) decreases the inverter voltage
b) increases the output voltage
c) switches the inverter stage between 0 to 1
d) does not switch the stage and keeps it stable

Answer: c
Explanation: Small disturbanes of noise switches the inverter stage between 0 and 1 or vice versa. It disturbs the normal operation or behaviour.

9. The buffer speeds up the
a) rise time
b) fall time

c) all of the mentioned
d) none of the mentioned

Answer: a
Explanation: The buffer speeds up the rise time of propogated signal edge. A buffer is the combination of two inverters in which one output is fed to the other as the input.

10. Overall delay increases as n
a) increases
b) decreases
c) exponentially decreases
d) logarithmically decreases

Answer: a
Explanation: Overall delay increases as n increases where n is the number of pass transistors connected in series.

Wiring Capacitances

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "Wiring Capacitances".

1. Which contribute to the wiring capacitance?
a) fringing fields
b) interlayer capacitance
c) peripheral capacitance
d) all of the mentioned

Answer: d
Explanation: The sources of capacitances which contribute to the total wiring capacitance are fringing field capacitance, interlayer capacitance and peripheral capacitance.

2. What does the value d in fringing field capacitance measures?
a) thickness of wire
b) length of the wire
c) wire to substrate separation
d) wire to wire separation

Answer: c
Explanation: The quantity d in fringing field capacitance measures the wire to substrate separation. It is the distance between the wire and the substrate used in the device.

3. Total wire capacitance is equal to
a) area capacitance
b) fringing field capacitance
c) area capacitance + fringing field capacitance
d) peripheral capacitance

Answer: c
Explanation: Total wire capacitance can be given as the sum of area capacitance and fringing field capacitance.

4. Interlayer capacitance occurs due to
a) separation between plates
b) electric field between plates
c) charges between plates
d) parallel plate effect

Answer: d
Explanation: Interlayer capacitance occurs due to parallel plate effect between one layer and another. When one capacitance value comes closer to another they create some combined effects.

5. Which capacitance must be higher?
a) metal to polysilicon capacitance
b) metal to substrate capacitance
c) metal to metal capacitance
d) diffusion capacitance

Answer: a
Explanation: Metal to polysilicon capacitance should be higher than metal to substrate capacitance. This is due to that when one layer underlies the other and in consequence interlayer capacitance is highly dependent on layout.

6. Peripheral capacitance is given in_____eper unit length
a) nano farad
b) pico farad
c) micro farad
d) farad

Answer: b
Explanation: Peripheral capacitance is given in picofarads per unit length. This is the sidewall capacitance. Each diode has this side wall capacitance.

7. For greater relative value of peripheral capacitance,_____should be small
a) source area
b) drain area
c) both of the mentioned
d) none of the mentioned

Answer: c
Explanation: The smaller the source or drain area, the greater the relative value of peripheral capacitance as they are both inversely related.

8. Diffusion capacitance is equal to
a) area capacitance
b) peripheral capacitance
c) fringing field capacitance
d) area capacitance + peripheral capacitance

Answer: d
Explanation: Diffusion capacitance is given by the sum of area capacitance and peripheral capacitance.

9. Polysilicon is suitable for
a) small distance
b) large distance
c) all of the mentioned'
d) none of the mentioned

Answer: a
Explanation: Polysilicon is unsuitable for routing Vdd or Vss other than for very small distance because of the relatively high Rs value of the polysilicon layer.

10. Which has high voltage drop?
a) metal layer
b) polysilicon layer
c) diffusion layer
d) silicide layer

Answer: b
Explanation: Polysilicon layer has high voltage drop. It has moderate RC product.

11. Which layer has high capacitance value?
a) metal
b) diffusion
c) silicide
d) polysilicon

Answer: b
Explanation: Diffusion or active layer has high capacitance value due to which it has low or moderate IR drop.

12. Which layer has high resistance value?
a) polysilicon
b) silicide
c) diffusion
d) metal

Answer: a
Explanation: Polysilicon layer has high resistance value and due to this it has high IR drop.

13. While measuring the output load capacitance Cgs,n and Cgs,p is not considered. Why?
a) Because Cgs,n and Cgs,p are the capacitances at the input nodes.
b) Because Cgs,n and Cgs,p does not exist during the operation of CMOS inverter
c) Because Cgs,n and Cgs,p are storing opposite charges and cancel out each other during calculation of load capacitance
d) None of the mentioned

Answer: a
Explanation: Cgs,n and Cgs,p are gate to source capacitances of nMOS and pMOS transistors in CMOS inverter. They are measured at input node. Therefore they are not considered for calculation of load capacitance.

14. During the calculation of load capacitance of a 1st stage CMOS inverter, the input node capacitances, Cgs,n and Cgs,p of the 2nd stage CMOS inverter is also considered.
a) True
b) False

Answer: b
Explanation: Instead thin oxide capacitance over the gate area is used for calculation.

Scaling Factors -1

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Scaling Factors - 1”.

1. Microelectronic technology cannot be characterized by
a) minimum feature size
b) power dissipation
c) production cost
d) designing cost

Answer: d
Explanation: Microelectronic technology can be characterized by minimum feature size, number of gates on one chip, power dissipation, die size, production cost etc and not by designing cost.

2. Which model is used for scaling?
a) constant electric scaling
b) constant voltage scaling
c) costant electric and voltage scaling
d) costant current model

Answer: c
Explanation: Constant electric scaling model and constant voltage scaling model is used for scaling.

3. α is used for scaling
a) linear dimensions
b) vdd
c) oxide thickness
d) non linear

Answer: a
Explanation: α is used as the scaling factor for linear dimensions where as β is used for supply voltage Vdd, gate oxide thickness etc.

4. For constant voltage model,
a) $\alpha = \beta$
b) $\alpha = 1$
c) $\alpha = 1/\beta$
d) $\beta = 1$

Answer: d
Explanation: For constant voltage model, $\beta = 1$ and $1/\beta$ is choosen for the scaling for all voltages.

5. For constant electric field model,
a) $\beta = \alpha$
b) $\alpha = 1$
c) $\alpha = 1/\beta$
d) $\beta = 1$

Answer: a
Explanation: For constant voltage model, $\beta = \alpha$.

6. Gate area can be given as
a) L/W
b) L * W
c) 2L/W
d) L/2W

Answer: b
Explanation: Gate area Ag can be given as the product of length and the width of the channel.

7. Gate area is scaled by
a) α
b) $1/\alpha$
c) $1/\alpha^2$
d) α^2

Answer: c
Explanation: Gate area is given as the product of length and width of the channel and it can be scaled by $1/\alpha^2$.

8. Gate capacitance per unit area is scaled by
a) α
b) 1
c) $1/\beta$
d) β

Answer: d
Explanation: Gate capacitance per unit area is scaled by β and this is given by €ox/D.

9. Parasitic capacitance is given by
a) Ax/d
b) Ax * d
c) d/Ax
d) Ax

Answer: a
Explanation: Parasitic capacitance is given by Ax/d where Ax is the area of the depletion region and d is the depletion width.

10. Parasitic capacitance is scaled by
a) β
b) 1/β
c) α
d) 1/α

Answer: d
Explanation: Parasitic capacitance is scaled by 1/α because area is scaled by 1/α^2 and d by 1/α. Thus (1/α^2)/(1/α) we will get 1/α.

Scaling Factors -2

This set of VLSI Interview Questions and Answers for freshers focuses on “Scaling Factors -2”.

1. Carrier density is scaled by
a) α
b) β
c) 1
d) α^2

Answer: c
Explanation: Carrier density in channel Qon is scaled by 1. Carrier density is given by C0*Vgs where C0 is scaled by β and Vgs is scaled by 1/β.

2. Channel resistance Ron is scaled by
a) α
b) β
c) 1
d) α^2

Answer: c
Explanation: Channel resistance Ron is scaled by 1. Channel resistance is given by (L/W)*(1/Qonμ).

3. Gate delay is given by
a) Ron/Cg
b) Ron * Cg
c) Cg/Ron
d) Cg^2 /Ron

Answer: b
Explanation: Gate delay Td is given as the product of Ron, channel resistance and Cg the gate capacitance.

4. Maximum operating frequency is scaled by
a) α/β
b) β/α
c) α^2 /β
d) β^2 /α

Answer: c
Explanation: Maximum operating frequency f0 is scaled by α^2/β. This is given by (W/L)*(μ*C0*Vdd/Cg).

5. Saturation current is scaled by
a) α
b) β
c) 1/α
d) 1/β

Answer: d
Explanation: Saturation current Idss is scaled by 1/β. This is given by $(Co*\mu/2)*W/L*(Vgs-Vt)^2$.

6. Vgs is scaled by
a) α
b) β
c) 1/α
d) 1/β

Answer: d
Explanation: Gate to source voltage Vgs is scaled by 1/β. All voltages are scaled by 1/β.

7. Current density J is scaled by
a) α/β
b) β/α
c) α^2/β
d) β^2/α

Answer: c
Explanation: Current density J is scaled by α^2/β. Current density is given by Idss/A where Idss is scaled by 1/β and area A by 1/α^2.

8. Power dissipation per gate is scaled by
a) $1/\alpha$
b) $1/\beta$
c) $1/\alpha^2$
d) $1/\beta^2$

Answer: d
Explanation: Power dissipation per gate is scaled by 1/β^2. This is the sum of static component Pgs and dynamic component Pgd.

9. Power dissipation per unit area is scaled by
a) $1/\alpha$
b) $1/\beta$
c) β^2/α^2
d) α^2/β^2

Answer: d
Explanation: Power dissipation per unit area Pa is scaled by α^2/β^2. This is given by Pg/Ag where Pg is scaled by $1/\beta^2$ and Ag by $1/\alpha^2$.

10. In constant voltage model, the saturation current is scaled by
a) α
b) β
c) 1
d) β^2

Answer: c
Explanation: Saturation current is scaled by 1 in constant voltage model. This is because saturation current is scaled by 1/β and here in constant voltage model β is 1.

11. In constant field model, maximum operationg frequency is scaled by
a) α
b) β
c) α^2
d) β^2

Answer: a
Explanation: In constant field model, maximum operating frequency is scaled by α. Maximum operating frequency is scaled by α^2/β and here in this model $\beta = \alpha$.

12. In constant electric field model, power dissipation per unit area is scaled by
a) α
b) β
c) 1
d) β^2

Answer: c
Explanation: Power dissipation per unit area is scaled by 1 in constant electric field model. This is scaled by α^2/β^2 and here in constant electric field model $\beta = \alpha$.

Switch Logic

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "Switch Logic".

1. The subsystem of the circuits should have_____interdependence
a) minimum
b) maximum
c) no
d) more

Answer: a
Explanation: The subsystem of the circuit or system to be designed should have minimum interdependence and complexity.

2. Switch logic is based on
a) pass transistors
b) transmission gates
c) pass transistors and transmission gates
d) design rules

Answer: c
Explanation: Switch logic is based on pass transistors or transmission gates. Pass transistor describes several logic families used in the design of integrated circuits. This logic reduces the count of transistors used to make different logic gates, by eliminating redundant transistors.

3. The switch logic approach takes_____static current
a) low
b) more
c) no
d) very less

Answer: c
Explanation: The switch logic approach takes no static current from the supply rails and is faster for small arrays.

4. Power dissipation in switch logic is
a) less
b) more
c) high
d) very less

Answer: a
Explanation: Power dissipation is small in switch logic approach since current only flows on switching.

5. Features of switch logic approach
a) occupies more area
b) no undesirable threshold voltage
c) low power dissipation
d) all of the mentioned

Answer: d
Explanation: Some of the features of switch logic approach are that it occupies more area, eliminates undesirable threshold voltage and has low power dissipation.

6. Pass transistor can be driven through_____pass transistors
a) one
b) no
c) more
d) two

Answer: b
Explanation: Pass transistor input should not be driven through any other pass transistors because there occurs loss in logic levels.

7. Basic AND and OR gate combinations are used in switch logic.
a) true
b) false

Answer: a
Explanation: Basic AND and OR combination of switches are possible and are used in switch logic. It is simple to design and easier.

8. When one pass transistor is driven using another, threshold voltage
a) affects
b) does not affect

Answer: a
Explanation: When logic levels are propogated through pass transistors are degraded by threshold voltage.

9. Switch logic approach is fast for
a) large arrays
b) small arrays
c) very large arrays
d) not at all fast for any type

Answer: b
Explanation: Switch logic approach is fast for smaller arrays and as the arrays becomes larger more switches and gates are requires which makes it a bit slower and complex.

10. Switch logic is designed using
a) complementary switches
b) silicon plates
c) conductors
d) resistors

Answer: a
Explanation: Switch logic is designed using n or p pass transistors or from complementary switches.

Gate Logic

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Gate Logic”.

1. Gate logic is also called as
a) transistor logic
b) switch logic
c) complementary logic
d) restoring logic

Answer: d
Explanation: Gate logic is also called as restoring logic. This is a logic circuitry designed so that even with an imperfect input pulse a standard output occurs at the exit of each successive logic gate.

2. Both NAND and NOR gates can be used in gate logic.
a) true
b) false

Answer: a
Explanation: Both NAND and NOR gates can be used in gate logic along with CMOS and AND and OR logic can be used in switch logic.

3. The CMOS inverter has_____power dissipation
a) low
b) more
c) no
d) very less

Answer: c
Explanation: The CMOS inverter has no static current and no power dissipation. Static charge remains until it is able to move away by means of electric discharge.

4. As the number of inputs increases, the NAND gate delay
a) increases
b) decreases
c) does not vary
d) exponentially decreases

Answer: a
Explanation: As the number of inputs increases, the NAND gate delay also increases because computation considering or using each input additional time is needed.

5. NAND gate delay can be given as
a) Ƭ int
b) Ƭ int/n
c) n*Ƭ int
d) 2n*Ƭ int

Answer: c
Explanation: NAND gate delay can be given as the product of number of inputs n and the nMOS inverter delay Ƭ int.

6. In CMOS NAND gate, p transistors are connected in
a) series
b) parallel
c) cascade
d) random

Answer: b
Explanation: In CMOS NAND gate, p transistors are connected in parallel but once again the geometries may require thought when several inputs are required.

7. BiCMOS is used for_____fan-out
a) less
b) more
c) no
d) very less

Answer: b
Explanation: BiCMOS NAND can be used when large fan-out is necessary. Fan-out is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed.

8. Which can handle high capacitance load?
a) NAND
b) nMOS NAND
c) CMOS NAND
d) BiCMOS NAND

Answer: d
Explanation: BiCMOS NAND can handle high capacitance load. It is more complex and it can handle high capacitance load such as in the I/O region of a chip.

9. Which gate is faster?
a) AND
b) NAND
c) NOR
d) OR

Answer: c
Explanation: NOR gate is faster. NAND is more complex than NOR and thus NOR is faster and efficient.

10. For a pseudo nMOS design the impedance of pull up and pull down ratio is
a) 4:1
b) 1:4
c) 3:1
d) 1:3

Answer: c
Explanation: For a pseudo nMOS design, the ratio of Zp.u. and Zp.d. is 3:1.

CMOS Logics

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "CMOS Logics".

1. In Pseudo-nMOS logic, n transistor operates in
a) cut off region
b) saturation region
c) resistive region
d) non saturation region

Answer: b
Explanation: In Pseudo-nMOS logic, n transistor operates in saturation region and p transistor operates in resistive region.

2. The power dissipation in Pseudo-nMOS is reduced to about_____compared to nMOS device
a) 50%
b) 30%
c) 60%

d) 70%

Answer: c
Explanation: The power dissipation in Pseudo-nMOS is reduced to about 60% compared to nMOS device.

3. Pseudo-nMOS has higher pull-up resistance than nMOS device.
a) true
b) false

Answer: a
Explanation: Pseudo-nMOS has higher pull-up resistance than nMOS device and thus inverter pair delay is larger.

4. In dynamic CMOS logic_____is used
a) two phase clock
b) three phase clock
c) one phase clock
d) four phase clock

Answer: d
Explanation: In dynamic CMOS logic, four phase clock is used in which actual signals are used to derive the clocks.

5. In clocked CMOS logic, output in evaluated in
a) on period
b) off period
c) both periods
d) half of on period

Answer: a
Explanation: In clocked CMOS logic, the logic is evaluated only in the on period of the clock. And owing to the extra transistor in series, slower rise time and fall times are expected.

6. In clocked CMOS logic, rise time and fall time are
a) faster
b) slower
c) faster first and then slows down
d) slower first and then speeds up

Answer: b
Explanation: In clocked CMOS logic, rise time and fall time are slower because of more number of transistors in series.

7. In CMOS domino logic_____is used
a) two phase clock
b) three phase clock
c) one phase clock
d) four phase clock

Answer: c
Explanation: In CMOS domino logic, single phase clock is used. Clock signals distributed on one wire is called as single or one phase clock.

8. CMOS domino logic is same as_____with inverter at the output line
a) clocked CMOS logic
b) dynamic CMOS logic
c) gate logic
d) switch logic

Answer: b
Explanation: CMOS domino logic is same as that of the dynamic CMOS logic with inverter at the output line.

9. CMOS domino logic occupies
a) smaller area
b) larger area
c) both of the mentioned
d) none of the mentioned

Answer: a
Explanation: CMOS domino logic structure occupies smaller area than conventional CMOS logic as only n-block is used.

10. CMOS domino logic has
a) smaller parasitic capacitance
b) larger parasitic capacitance
c) low operating speed
d) very large parasitic capacitance
Answer: a
Explanation: CMOS domino logic has smaller parasitic capacitance and higher operating speed.

11. In CMOS domino logic_____is possible
a) inverting structure
b) non inverting structure
c) inverting and non inverting structure
d) very complex design

Answer: b
Explanation: In CMOS domino logic, only non inverting structures are possible because of the presence of the inverting buffer.

Clocked Sequential Circuits

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "Clocked Sequential Circuits".

1. Clocked sequential circuits are
a) two phase overlapping clock
b) two phase non overlapping clock
c) four phase overlapping clock
d) four phase non overlapping clock

Answer: b
Explanation: Clocked sequential circuits are two phase non overlapping clock signal. Clock signals are distributed in two wires and it is non overlapping.

2. Which are easier to design?
a) clocked circuits
b) asynchronous sequential circuits
c) clocked circuits with buffer
d) asynchronous sequential circuits with buffers

Answer: a
Explanation: Clocked circuitry are easier to design than the asynchronous sequential circuits. But it is slower than the asynchronous sequential circuit.

3. _____is used to drive high capacitance load
a) single polar capability
b) bipolar capability
c) tripolar capability
d) bi and tri polar capability

Answer: b
Explanation: Bipolar capability is used to drive high capacitance load. It can handle high loads as it is done by BiCMOS NAND gate logic.

4. As the temperature is increased, storage time _____
a) halved
b) doubled
c) does not change
d) tripled

Answer: a
Explanation: As the temperature is increased, storage time is halved. It is inversely proportional to the storage time.

5. Inverting dynamic register element consists of_____transistors for nMOS and_____for CMOS
a) two, three
b) three, two
c) three, four
d) four, three

Answer: c
Explanation: Dynamic register element consists of three transistors for nMOS and four for CMOS.

6. Non inverting dynamic register storage cell consists of_____transistors for nMOS and _____ for CMOS
a) six, eight
b) eight, six
c) five, six
d) six, five

Answer: a
Explanation: Non inverting dynamic register storage cell consists of six transistors for nMOS and eight for CMOS.

7. Register cell consists of
a) inverter
b) pass transistor
c) both of the mentioned
d) none of the mentioned

Answer: c
Explanation: Register cell consists of an inverter and a pass transistor or a transmission gate. Dynamic register cell consists of stick/circuit notation.

8. In a four bit dynamic shift register basic nMOS transistor or inverters are connected in
a) series
b) cascade
c) parallel
d) series and parallel

Answer: b
Explanation: The basic inverters or nMOS transistors are connected in cascade to obtain four bit dynamic shift register.

9. In four bit dynamic shift register output is obtained
a) parallel output at inverters 1,3,5,7
b) parallel output at inverters 1,5,8
c) parallel output at all inverters
d) parallel output at inverter 2,4,6,8

Answer: d
Explanation: In four bit dynamic shift register , output is obtained parallely at inverters 2,4,6,8.

10. For signals which are updated frequently_____ is used
a) static storage
b) dymanic storage
c) static and dynamic storage
d) buffer

Answer: b
Explanation: For signals which are updated frequently dynamic storage elements are used. It can be done at < 0.25 msec interval.

Floor Layout

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Floor Layout”.

1. A 4-bit processor has two buses which are
a) unidirectional
b) bidirectional

c) one unidirectional and one bidirectional
d) more than two buses

Answer: c
Explanation: A 4-bit processor has two buses one is bidirectional to carry operand and output to shifter and register array and another bus unidirectional to carry input.

2. The IN and OUT bus lines relative positions are interchanged to
a) match height
b) match length
c) match width
d) match thickness

Answer: a
Explanation: The IN and OUT bus line's relative positions are interchanged to make the cell stretchable and to match the height of the block and spacings.

3. The IN and OUT bus lines should be in
a) metal
b) polysilicon
c) diffusion
d) silicon

Answer: a
Explanation: The IN and OUT bus lines should be in metal rather than diffusion or polysilicon to mate with the bus structures of other blocks.

4. Extensions are
a) vertical
b) horizontal
c) diagonal
d) happazard

Answer: b
Explanation: Extensions are horizontal or parallel to the stratified unit and rifts are described as extension zones.

5. Rifts and extensions should be placed in
a) minimum amount of geometry
b) maximum amount of geometry
c) in slopes

d) anywhere in the layout

Answer: a
Explanation: Rifts and extensions should be placed where they cut a minimum amount of simple geometry, one in polysilicon and one in diffusion.

6. Rifts are used for smooth flow through buses.
a) true
b) false

Answer: a
Explanation: Rifts are used for smooth flow through buses as suggested and hence one in used in polysilicon and other in diffusion.

7. Input and output pads are made up of
a) polysilicon
b) metal
c) silicon
d) carbon

Answer: b
Explanation: Input and output pads are made up of metal and it used to connect chips from one circuitry to another.

8. Bonding pads are placed
a) in the chip
b) exactly at the centre of chip
c) edge of the chip
d) above the chip

Answer: c
Explanation: Bonding pads are positioned near to the edge of the chips although there will be a Vdd bus between bonding pads and chip boundary.

9. Which pad contains Schmitt trigger circuitry?
a) Vdd pads
b) Vss pads
c) input pads
d) output pads

Answer: c
Explanation: Input pad contains over voltage protection features and also contains inverting circuitry or Schmitt trigger circuitry.

10. Which occupies lesser area?
a) Vdd pads
b) Vss pads
c) input pads
d) output pads

Answer: d
Explanation: Output pads provide large current for off-wiring and also inputs to other devices. But these pads uses minimum space.

Built-in Self Test

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on "Built-in Self Test".

1. Built-in self test aims to
a) reduce test pattern generation cost
b) reduce volume of test data
c) reduce test time
d) all of the mentioned

Answer: d
Explanation: Built-in self test objectives are to reduce test pattern generation cost, to reduce volume of test data and to reduce test time.

2. In data compression technique, comparison is done on
a) test response
b) entire test data
c) data inputs
d) output sequences

Answer: a
Explanation: In data compression technique, comparison is made on compacted test response instead on entire test data.

3. Signature analysis performs
a) addition
b) multiplication

c) polynomial division
d) amplifies

Answer: c
Explanation: Signature analysis performs polynomial division that is division of data out of the device under test.

4. The signature analysis method can be represented mathematically as
a) R(x) = P(x) * C(x)
b) R(x) = P(x) / C(x)
c) R(x) = C(x) / P(x)
d) R(x) = C(x) * P(x)

Answer: b
Explanation: The signature analysis method is represented mathematically as R(x) = P(x) / C(x) where R(x) is the signature, C(x) is characteristic polynomial.

5. Transition counting does the count of transition only in one specific direction at a time.
a) true
b) false

Answer: a
Explanation: Transition counting does the count of transition in specified direction (0 t0 1 or 1 to 0).

6. BILBO uses only signature analysis.
a) true
b) false

Answer: b
Explanation: Built-in logic block observer method uses signature analysis in conjunction with a scan path.

7. In which mode, storage elements are used independently?
a) normal mode
b) test 1 mode
c) test 2 mode
d) final mode

Answer: a
Explanation: In normal mode, storage elements are used independently and in this mode signal B1=B2=1.

8. Storage elements are connected as a serial shift register when
a) B1=B2=1
b) B1=B2=0
c) B1=0,B2=1
d) B1=1,B2=0

Answer: b
Explanation: When B1=B2=0, storage elements are configured as scan path, they are connected as serial shift register.

9. The circuit is configured as LFSR, when
a) B1=B2=1
b) B1=B2=0
c) B1=0, B2=1
d) B1=1, B2=0

Answer: d
Explanation: When B1=1 and B2=0, the circuit is configured as LFSR mode and can be used as either polynomial divider or random test pattern generator.

10. The BILBO is reset, when
a) B1=B2=1
b) B1=B2=0
c) B1=0, B2=1
d) B1=1, B2=0

Answer: c
Explanation: When B1=0 and B2=1, in the final mode, the BILBO is reset.

11. Self-checking technique consists of
a) supplying coded input data
b) receiving coded output data
c) supplying all possible input sequence
d) all of the mentioned

Answer: a
Explanation: Self-checking technique consists of supplying coded input data to the logic block under test and comparing the output.

12. The type of error in self-checking technique are
a) simple error
b) unidirectional error
c) multiple error
d) all of the mentioned

Answer: d
Explanation: The type of error in self-checking techniques are simple errors, unidirectional errors and multiple errors.

13. The parity check detection is done using
a) OR gate
b) AND gate
c) XOR gate
d) NOR gate

Answer: c
Explanation: The parity check detects simple errors using XOR gates and for each type of error, approximate coding technique is used.

14. Which errors are detected using duplication codes?
a) single errors
b) unidirectional errors
c) bidirectional errors
d) multiple errors

Answer: d
Explanation: Multiple errors are detected using duplication codes which consists of duplicating the information.

MOS Transistor Threshold Voltage

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “MOS Transistor Threshold Voltage”.

1. The electrical equivalent component for MOS structure is:
a) Resistor

b) Capacitor
c) Inductor
d) Switch

Answer: b
Explanation: The MOS structure acts as a capacitor with metal gate and semiconductor acting as parallel plate conductors and oxide as dielectric between them.

2. The Fermi potential is the function of:
a) Temperature
b) Doping concentration
c) Difference between Fermi level and intrinsic Fermi level
d) All of the mentioned

Answer: d
Explanation: The Fermi potential, which is a function of temperature and doping, denotes the difference between the intrinsic Fermi level and the Fermi level.

3. The direction of electric field when the gate voltage is zero:
a) Metal to semiconductor
b) Semiconductor to metal
c) No electric field exists
d) None of the mentioned

Answer: a
Explanation: Metal being more positive compared to semiconductor.. Electric field exists from metal to semiconductor.

4. Consider a MOS structure with equilibrium Fermi potential of the doped silicon substrate is given as 0.3eV. Electron affinity of Si is 4.15eV and metal is 4.1eV. Find the built in potential of the MOS system:
a) -0.8eV
b) 0.8eV
c) 0.9eV
d) -0.9eV

Answer: d
Explanation: Surface potential: $q\Phi s = 4.15eV+0.55eV+0.3eV=5.0eV$
$q\Phi m-q\Phi s = 4.1eV – 5.0eV =-0.9eV.$

5. When gate voltage is negative for enhancement mode n-MOS, the direction of electric field will be:

a) Metal to semiconductor
b) Semiconductor to metal
c) No field exists
d) None of the mentioned

Answer: b
Explanation: When gate voltage is negative, holes in substrate are attracted towards surface creating electric field from semiconductor to metal.

6. At threshold Voltage, the surface potential is:
a) – Fermi potential
b) Fermi potential
c) 2 Fermi potential
d) -2 Fermi potential

Answer:a
Explanation: When surface potential reaches –fermi potential, the surface inversion occurs. The gate voltage which brings these changes is known as threshold voltage.

7. Surface inversion occurs when gate voltage is:
a) Less than zero
b) Less than threshold voltage
c) Equal to threshold voltage
d) Greater than threshold voltage

Answer: c
Explanation: Surface inversion occurs when gate voltage is equal to threshold voltage.

9. For enhancement mode n-MOSFET, the threshold voltage is:
a) Equal to 0
b) Greater than zero or Positive quantity
c) Negative voltage or lesser than zero
d) All of the mentioned

Answer: b
Explanation: For enhancement mode n-MOSFET, the threshold voltage is positive quantity.

10. The threshold voltage depends on:
a) The workfunction difference between gate and channel
b) The gate voltage component to change surface potential
c) The gate voltage component to offset the depletion charge and fixed charges in gate oxide

d) All of the mentioned

Answer: d
Explanation: The threshold voltage depends on: The workfunction difference between gate and channel, The gate voltage component to change surface potential, The gate voltage component to offset the depletion charge and fixed charges in gate oxide

Noise Margin

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Noise Margin”.

1. Noise Margin is :
a) Amount of noise the logic circuit can withstand
b) Difference between VOH and VIH
c) Difference between VIL and VOL
d) All of the Mentioned

Answer: d
Explanation: Noise Margin is defined as the amount of noise the logic circuit can withstand, it is given by difference between VOH and VIH or VIL and VOL.

2. The VIL is found from transfer characteristic of inverter by:
a) The point where straight line at VOH ends
b) The slope of the transition at a point at which the slope is equal to -1
c) The midpoint of the transition line
d) All of the mentioned

Answer: b
Explanation: The VIL is the input voltage at which the slope of the transition will be equal to -1.

3. The VIH is found from transfer characteristic of inverter by:
a) The point where straight line at VOH ends
b) The slope of the transition at a point at which the slope is equal to -1
c) The midpoint of the transition line
d) All of the mentioned

Answer: b
Explanation: The VIH is the input voltage at which the slope of the transition will be equal to -1. In Transfer characteristics at 2 points we will find the slope to be -1.

4. The relation between threshold voltage and Noise Margin is:
a) Vth = sqrt(Noise Margin)
b) Vth = NMH – NML
c) Vth = (NMH+NML)/2
d) None of the metioned

Answer: d
Explanation: None.

5. The Lower Noise Margin is given by:
a) VOL – VIL
b) VIL – VOL
c) VIL ~ VOL(Difference between VIL and VOL, depends on which one is greater)
d) All of the Mentioned

Answer: b
Explanation: Noise margin = VIL-VOL.

6. The Higher Noise Margin is given by:
a) VOH – VIH
b) VIH – VOH
c) VIH ~ VOH(Difference between VIH and VOH, depends on which one is greater)
d) All of the mentioned

Answer: a
Explanation: Noise margin =VOH – VIH.

7. The Uncertain or transition region is between:
a) VIH and VOH
b) VIL and VOL
c) VIH and VIL
d) VOH and VOL

Answer: c
Explanation: In Input the uncertain region is VIH and VIL.

8. The noise immunity _____with noise margin
a) Decreases
b) Increases
c) Constant
d) None of the Mentioned

Answer: b
Explanation: The noise immunity is directly proportional to noise margin.

9. If VIL of the 2nd gate is higher than VOL of the 1st gate, then logic output 0 from the 1st gate is considered as :
a) Logic input 1
b) Uncertain
c) Logic input 0
d) None of the mentioned

Answer: c
Explanation: Logic output 0 from first gate is considered as logic input 0 at second gate as it lies within the range.

10. If VIL of the 2nd gate is lower than VOL of the 1st gate, then logic output 0 from the 1st gate is considered as :
a) Logic input 1
b) Uncertain
c) Logic input 0
d) None of the mentioned

Answer: b
Explanation: The level of output signal from 1st gate is higher than the range for low input at 2nd gate. So it is uncertain.

11. Input Voltage between VIL and VOL is considered as:
a) Logic Input 1
b) Logic Input 0
c) Uncertain
d) None of the mentioned

Answer: b
Explanation: None.

12. If VIH of the 2nd gate is higher than VOH of the 1st gate, then logic output 0 from the 1st gate is considered as :
a) Logic input 1
b) Uncertain
c) Logic input 0
d) None of the mentioned

Answer: b
Explanation: The level of output signal from 1st gate is higher than the range for low input at 2nd gate. So it is uncertain.

Test Patterns

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Test Patterns “.

1. Which method is used to determine structural defects?
a) deterministic test pattern
b) algorithmic test pattern
c) random test pattern
d) exhaustive test pattern

Answer: a
Explanation: Deterministic test pattern are used to detect specific faults or structural faults for a circuit under test.

2. Which is known as stored test pattern method?
a) deterministic test pattern
b) algorithmic test pattern
c) random test pattern
d) exhaustive test pattern

Answer: a
Explanation: Deterministic test pattern method is also known as stored test pattern method in the context of BIST applications.

3. Which method uses finite state machine for developing the test pattern?
a) deterministic test pattern
b) algorithmic test pattern
c) random test pattern
d) exhaustive test pattern

Answer: b
Explanation: Algorithmic test pattern method uses the hardware finite state machine for generating algorithmic test vectors for the circuit under test.

4. A n-bit counter produces_____number of total input combinations
a) $2^{(n-1)}$
b) $2^{(n+1)}$

c) 2^n
d) 2n

Answer: c
Explanation: A n-bit counter produces totally 2^n number of all possible input combinations for testing the circuit under test and it is called as exhaustive test pattern method.

5. Exhaustive test pattern determines
a) gate level faults
b) logic level faults
c) functional faults
d) structural faults

Answer: a
Explanation: Exhaustive test pattern method detects all gate level struck-at fault and also bridging fault.

6. Exhaustive test pattern also detects delay faults.
a) true
b) false

Answer: b
Explanation: Exhaustive test pattern method does not detect all transistor level faults or delay faults since those faults needs specific ordering.

7. Which is not suitable for circuits having large N values?
a) exhaustive test pattern method
b) pseudo-exhaustive test pattern method
c) random test pattern method
d) deterministic test pattern method

Answer: a
Explanation: Exhaustive test pattern method is not suitable for circuit having large N values since there is a limit for fault coverage.

8. Which method needs fault simulation?
a) exhaustive test pattern method
b) pseudo-exhaustive test pattern method
c) random test pattern method
d) deterministic test pattern method

Answer: a
Explanation: Exhaustive test pattern method needs fault simulation for determining fault coverage where as pseudo-exhaustive test pattern method does not need fault simulation.

9. In which method sequences are repeatable?
a) exhaustive test pattern method
b) pseudo-exhaustive test pattern method
c) random test pattern method
d) pseudo-random test pattern method

Answer: d
Explanation: Pseudo-random test pattern method have properties similar to random pattern sequence but the sequence are repeatable.

10. Which method is used for external functional testing?
a) exhaustive test pattern method
b) pseudo-exhaustive test pattern method
c) random test pattern method
d) pseudo-random test pattern method

Answer: c
Explanation: Random test pattern method is used for external functional testing of microprocessors as well as in ATPG software.

Fault Models

This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Fault Models “.

1. Which are processing faults?
a) missing contact window
b) parasitic transistor
c) oxide breakdown
d) all of the mentioned

Answer: d
Explanation: Some of the real defects in chip such as processing faults are missing contact window, parasitic transistor and oxide breakdown.

2. Surface impurities occurs due to ion migration.
a) true

b) false

Answer: a
Explanation: Some of the material defects are bulk defects and surface impurities. Bulk defects are cracks and crystal imperfection and surface impurities occurs due to ion migration.

3. Electromigration is a
a) processing fault
b) material defects
c) time dependent failure
d) packaging fault

Answer: c
Explanation: Different types of real defects in chips are processing fault, material defects, time dependent failure and packaging fault. Time dependent failures are dielectric breakdown and electromigration.

4. Which relation is correct?
a) failure – error – fault
b) fault – error – failure
c) error – fault – failure
d) error – failure – fault

Answer: b
Explanation: The relation fault – error – failure is correct. Error is caused by faults and failure which is a deviation of the circuit is caused by error.

5. For a circuit with k lines,_____single stuckat fault is possible
a) k
b) 2k
c) k/2
d) k^2

Answer: b
Explanation: For a circuit with k lines, 2k single stuck-at faults are possible and 3^k – 1 multiple stuck-at faults are possible.

6. Single stuck-at fault is technology independent.
a) true
b) false

Answer: a
Explanation: Single stuck-at fault is technology independent. It can be applied to TTL, CMOS etc. It is also design style independent.

7. For a n signal lines circuit, _____ bridging faults are possible
a) n
b) 2n
c) n^2
d) n/2

Answer: c
Explanation: For circuit with n lines, n^2 bridging faults are possible. Bridging fault occurs when two lines are connected when they should not be connected. It leads to wired AND or wired OR.

8. IDDQ fault occurs when there is
a) increased voltage
b) increased quiescent current
c) increased power supply
d) increased discharge

Answer: b
Explanation: When input is low, both P and N transistors are conducting causing increase in quiescent current which leads to IDDQ fault.

9. Which fault causes output floating?
a) stuck-open
b) stuck-at
c) stuck-on
d) IDDQ

Answer: a
Explanation: Transistor with stuck-open fault causes output floating. Stuck-open faults requires two vector tests.

10. Data retention time comes under _____ fault
a) functional fault
b) memory fault
c) parametric fault
d) structural fault

Answer: c
Explanation: One of the memory faults is parametric fault. Some of the parametric faults are noise margin, data retention time, power consumption, output levels etc.

11. In PLA, missing cross point in OR-array leads to
a) OR fault
b) growth fault
c) missing fault
d) disapperance fault

Answer: d
Explanation: In PLA, missing cross point in AND array leads to growth fault and missing cross point in OR-array leads to disapperance fault.

12. In PLA, extra crosspoint in AND-array leads to
a) OR fault
b) growth fault
c) missing fault
d) disapperance fault

Answer: d
Explanation: In PLA, extra crosspoint in AND-array leads to shrinkage or disapperance fault whereas extra crosspoint in OR-array leads to appearance fault.

13. The number of paths_____with number of gates
a) increases exponentially
b) decreases exponentially
c) remains the same
d) increases rapidly

Answer: a
Explanation: The number of paths increases exponentially with number of gates. Propogation delay of the path exceeds the clock interval.

14. The quality of the test set is measured by
a) fault margin
b) fault detection
c) fault correction
d) fault coverage

Answer: d
Explanation: The quality of a test set is measured by its fault coverage. It gives the fraction of fault that are detected by the test set.