SYED AMMAL ENGINEERING COLLEGE

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EC6302-DIGITAL ELECTRONICS
2 MARKS QUESTIONS WITH ANSWER
UNIT I-MINIMIZATION TECHNIQUES AND LOGIC GATES

1. Define binary logic?

Binary logic consists of binary variables and logical operations. The variables are designated by the alphabets such as A, B, C, x, y, z, etc., with each variable having only two distinct values: 1 and 0. There are three basic logic operations: AND, OR, and NOT.

2. Convert (634) 8 to binary

Decimal	6	3	4
Binary	110	011	100

Answer = 110011100

3. State the different classification of binary codes?

1. Weighted codes
2. Non - weighted codes
3. Reflective codes
4. Sequential codes
5. Alphanumeric codes
6. Error Detecting and correcting codes.

4. State the steps involved in Gray to binary conversion?

The MSB of the binary number is the same as the MSB of the gray code number. So write it down. To obtain the next binary digit, perform an exclusive OR operation between the bit just written down and the next gray code bit.

5. Convert gray code 101011 into its binary equivalent.

Gray Code: 1 0 1 0 1 1
Binary Code: 1 1 0 0 1 0

6. Subtract (0 1 0 1) $_2$ from (1 0 1 1) $_2$

1 0 1 0
0 1 0 1
Answer = 0 11 0

7. List the different number systems?

Decimal Number system
Binary Number system
Octal Number system
Hexadecimal Number system

8. State the abbreviations of ASCII and EBCDIC code?

ASCII - American Standard Code for Information Interchange.
EBCDIC-Extended Binary Coded Decimal Information Code.

9. Write the names of basic logical operators.

NOT / INVERT, AND and OR

10. What are basic properties of Boolean algebra?

The basic properties of Boolean algebra are commutative property, associative Property and distributive property.

11. State the associative property of boolean algebra.

The associative property of Boolean algebra states that the OR ing of several variables results in the same regardless of the grouping of the variables. The associative property is stated as follows:

$$A+ (B+C) = (A+B) +C$$

12. State the commutative property of Boolean algebra.

The commutative property states that the order in which the variables are OR ed makes no difference. The commutative property is:

$$A+B=B+A$$

13. State the distributive property of Boolean algebra.

The distributive property states that AND ing several variables and OR ing the result with a single variable is equivalent to OR ing the single variable with each of the the several variables and then AND ing the sums.

The distributive property is: $A+BC= (A+B) (A+C)$

14. State the absorption law of Boolean algebra.

The absorption law of Boolean algebra is given by $X+XY=X$, $X(X+Y) =X$.

15. Simplify the following using De Morgan's theorem

[((AB)'C)" D]' [((AB)'C)" D]' = ((AB)'C)" + D' [(AB)' = A' + B']
= (AB)' C + D'
= (A' + B') C + D'

16. State De Morgan's theorem.

De Morgan suggested two theorems that form important part of Boolean algebra.
They are,

The complement of a product is equal to the sum of the complements.

$$(AB)' = A' + B'$$

The complement of a sum term is equal to the product of the complements.

$$(A + B)' = A'B'$$

17. Reduce A (A + B)

A (A + B) = AA + AB
= A (1 + B) [1 + B = 1]
= A.

18. Reduce A'B'C' + A'BC' + A'BC

A'B'C' + A'BC' + A'BC = A'C'(B' + B) + A'B'C

= A'C' + A'BC [A + A' = 1]
= A'(C' + BC)
= A'(C' + B) [A + A'B = A + B]

19. Reduce AB + (AC)' + AB'C (AB + C)

AB + (AC)' + AB'C (AB + C) = AB + (AC)' + AAB'BC + AB'CC
= AB + (AC)' + AB'CC [A.A' = 0]
= AB + (AC)' + AB'C [A.A = 1]
= AB + A' + C' =AB'C [(AB)' = A' + B']
= A' + B + C' + AB'C [A + AB' = A + B]
= A' + B'C + B + C' [A + A'B = A + B]
= A' + B + C' + B'C
= A' + B + C' + B'
= A' + C' + 1
= 1 [A + 1 =1]

20. Define duality property.

Duality property states that every algebraic expression deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are interchanged. If the dual of an algebraic expression is desired, we simply interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

21. Simplify the following expression

Y = (A + B) (A = C) (B + C)
= (A A + A C + A B + B C) (B + C)
= (A C + A B + B C) (B + C)
= A B C + A C C + A B B + A B C + B B C + B C C
= A B C

22. What are the methods adopted to reduce Boolean function?

i) Karnaugh map
ii) Tabular method or Quine Mc-Cluskey method
iii) Variable entered map technique.

23. What is a karnaugh map?

A karnaugh map or k map is a pictorial form of truth table, in which the map diagram is made up of squares, with each squares representing one minterm of the function.

24. What are called don't care conditions?

In some logic circuits certain input conditions never occur, therefore the corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or'd' in the truth tables and are called don't care conditions or incompletely specified functions.

25. What is a prime implicant?

A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.

26. What is an essential implicant?

If a min term is covered by only one prime implicant, the prime implicant is said to be essential

27. What is a Logic gate?

Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function.

28. Which gates are called as the universal gates? What are its advantages?

The NAND and NOR gates are called as the universal gates. These gates are used to perform any type of logic application.

29. Mention the important characteristics of digital IC's?

- Fan out
- Power dissipation
- Propagation Delay
- Noise Margin
- Fan In
- Operating temperature
- Power supply requirements

30. Define Fan-out?

Fan out specifies the number of standard loads that the output of the gate can drive with out impairment of its normal operation.

31. What is propagation delay?

Propagation delay is the average transition delay time for the signal to propagate from input to output when the signals change in value. It is expressed in ns.

32. Define noise margin?

It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. It is expressed in volts.

33. Define fan in?

Fan in is the number of inputs connected to the gate without any degradation in the voltage level.

34. What are the types of TTL logic?

Open collector output, Totem-Pole Output, Tri-state output.

35. Why totem pole outputs cannot be connected together.

Totem pole outputs cannot be connected together because such a connection might produce excessive current and may result in damage to the devices.

UNIT-II COMBINATIONAL CIRCUITS

1. Define combinational logic

When logic gates are connected together to produce a specified output for certain specified

combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

2. Explain the design procedure for combinational circuits

- The problem definition
- Determine the number of available input variables & required O/P variables
- Assigning letter symbols to I/O variables
- Obtain simplified Boolean expression for each O/P
- Obtain the logic diagram

3. What is a half-adder?

A half adder is an arithmetic circuit that adds two binary digits. It has two inputs and two outputs only (sum and carry)

4. What is a full-adder?

A full adder is an arithmetic circuit that adds two binary digits and a carry, i.e. Three bits. It has three inputs and two outputs (sum and carry)

5. What is a half-Subtractor?

A half-Subtractor is an arithmetic circuit that subtracts one binary digit form another. It has two inputs and two outputs (difference and borrow)

6. What is a full-Subtractor?

A full-Subtractor is an arithmetic circuit that subtracts one binary digit form another considering a borrow. It has three inputs and two outputs (Difference and Borrow)

7. Why are Subtractor ICs not available?

Since subtraction is performed using adders by making use of 1's and 2's complement methods, separate subtraction ICs are not available.

8. What is parallel adder?

A parallel adder is an arithmetic circuit that adds two numbers in parallel form.

9. What is carry propagation delay of a full-adder?

The carry propagation delay of a full-adder in a parallel adder is the time between the application of the carry-in and the occurrence of the carry-out.

10. What do you mean by cascading of parallel adders? Why it required?

Connecting the parallel adders in series, i.e. connecting the carry out of one parallel adder to the carry-in of another parallel adder is called cascading them. It is required when a large number or bits are to be added.

11. How is addition of large binary numbers accomplished?

The addition of large binary numbers can be accomplished by cascading two or more parallel adder chips.

12. What is a combinational logic circuit? Write an example.

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called 'Combinational logic circuit'. A combinational circuit consists of input variables, logic gates

and output variables. For example, consider following Boolean expression:

$$Y = AB + BC + AC$$

13. What is a half adder and a full adder?

Half adder: The logic circuit which performs the arithmetic sum of two bits is called a half adder.

Full adder: The logic circuit which performs the arithmetic sum of three bits (bit 1: input 1, bit 2:input 2, bit 3: carry from the previous addition) is called a full adder.

14. What is a ripple-carry-adder?

A ripple-carry – adder is parallel adder in which the carry-out of each full adder is the carry-in to the next most significant adder.

15. How does the look-ahead-carry speed up the addition process?

The Look-ahead-carry adder speeds up the addition process by eliminating the ripple carry delay. It examines all the input bits simultaneously and also generates the carry-in-bits for all the stages simultaneously.

16. What is a serial adder?

A serial adder is a sequential circuit used to add serially binary numbers.

17. Why does a serial adder require only one full-adder?

A serial adder requires only one full-adder because in this the bits are added Serially, i.e. one pair of bits at a time.

18. What is the drawback of serial adders? For which applications are they preferred?

The drawback of serial adder is the serial adders are slower than parallel adders. They are preferred for application where circuit minimization is more important than speed as in pocket calculators.

19. Why serial adders are slower than parallel adders?

Serial adders are slower than parallel adders because they require one clock pulse for each pair of bits added.

20. What are differences between serial and parallel adders?

The parallel adder uses registers with parallel load, whereas the serial adder uses shift registers. The number of full-adder circuits in the parallel adder is equal to the number of bits in the binary numbers, whereas the serial adder requires only full- adder circuits and a carry flip-flop. Excluding the registers, the parallel adder is combinational circuit, whereas the serial adder is a sequential circuit. The sequential circuit in the serial adder consist of full-adder and a flip-flop that stores the output carry.

21. In what way is a BCD adder different form a binary adder?

While adding BCD numbers, the output is required to be corrected which is not required in the case of binary adders.

22. Compare the hardware requirements of a BCD arithmetic unit and a straight binary arithmetic unit.

Because of the need for correction circuit, the BCD arithmetic unit requires more hardware

than the straight binary arithmetic unit.

23. Why is decimal 6 required to be added in a BCD adder if the sum is not a valid BCD number?

16 possible combinations are there with 4 bit number. In BCD only 10 of these are used and the other 6 are skipped. That is why 6 is required to be added.

24. What are code converters?

Code converters are logic circuits whose inputs are bit patterns representing numbers or characters in one code and whose outputs are the corresponding

25. What is a parity bit generator?

A parity bit generator is a digital circuit that generators a bit called the parity bit to be added to the data bits.

26. How is even parity bit generated for four data bits?

To generate an even parity bit for four data bits, the four data bits are added using three X-OR gates. The sum bit will be the parity bit.

27. How is odd parity bit generated for four data bits?

To generate an even parity bit for four data bits, the four data bits are added using three X-OR gates and the sum bit is inverted.

28. What is a comparator?

A comparator is a logic circuit that compares the magnitudes of two binary numbers. The EX–NOR gate(coincidence gate) is a basic comparator.

UNIT-III SEQUENTIAL CIRUITS

1. What are the classifications of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals into two types. They are,

1) Synchronous sequential circuit.
2) Asynchronous sequential circuit.

2. Define Flip flop.

The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.

3. What are the different types of flip-flop?

There are various types of flip flops. Some of them are mentioned below they are, RS flip-flop, SR flip-flop, D flip-flop, JK flip-flop, T flip-flop

4. What is the operation of RS flip-flop?

- When R input is low and S input is high the Q output of flip-flop is set.
- When R input is high and S input is low the Q output of flip-flop is reset.
- When both the inputs R and S are low the output does not change
- When both the inputs R and S are high the output is unpredictable.

5. What is the operation of SR flip-flop?

- When R input is low and S input is high the Q output of flip-flop is set.
- When R input is high and S input is low the Q output of flip-flop is reset.
- When both the inputs R and S are low the output does not change.
- When both the inputs R and S are high the output is unpredictable.

6. What is the operation of D flip-flop?

In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.

7. What is the operation of JK flip-flop?

- When K input is low and J input is high the Q output of flip-flop is set.
- When K input is high and J input is low the Q output of flip-flop is reset.
- When both the inputs K and J are low the output does not change
- When both the inputs K and J are high the output is toggle

8. What is the operation of T flip-flop?

- T flip-flop is also known as Toggle flip-flop.
- When T=0 there is no change in the output.
- When T=1 the output switch to the complement state (ie) the output toggles.

9. Define race around condition.

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called ‘race around condition’.

10. What is edge-triggered flip-flop?

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

11. What is a master-slave flip-flop?

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.

12. Define rise time.

The time required to change the voltage level from 10% to 90% is known as rise time(tr).

13. Define fall time.

The time required to change the voltage level from 90% to 10% is known as fall time(tf).

14. Define skew and clock skew.

The phase shift between the rectangular clock waveforms is referred to as skew and the time delay between the two clock pulses is called clock skew.

15. Define setup time.

The setup time is the minimum time required to maintain a constant voltage levels at the excitation inputs of the flip-flop device prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as setup.

16. Define hold time.

The hold time is the minimum time for which the voltage levels at the excitation inputs must remain constant after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as thold .

17. Define propagation delay.

A propagation delay is the time required to change the output after the application of the input.

18. Define registers.

A register is a group of flip-flops flip-flop can store one bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

19. Define shift registers.

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.

20. What are the different types of shift type?

There are five types. They are Serial In Serial Out Shift Register, Serial In Parallel Out Shift Register, Parallel In Serial Out Shift Register, Parallel In Parallel Out Shift Register and Bidirectional Shift Register.

21. Explain the flip-flop excitation tables for RS FF.

In RS flip-flop there are four possible transitions from the present state to the next state. They are,

0-0 transition: This can happen either when R=S=0 or when R=1 and S=0.
0-1 transition: This can happen only when S=1 and R=0.
1-0 transition: This can happen only when S=0 and R=1.
1-1 transition: This can happen either when S=1 and R=0 or S=0 and R=0.

22. Explain the flip-flop excitation tables for JK flip-flop

In JK flip-flop also there are four possible transitions from present state to next state. They are,

0-0 transition: This can happen when J=0 and K=1 or K=0.
0-1 transition: This can happen either when J=1 and K=0 or when J=K=1.
1-0 transition: This can happen either when J=0 and K=1 or when J=K=1.
1-1 transition: This can happen when K=0 and J=0 or J=1.

23. Explain the flip-flop excitation tables for D flip-flop

In D flip-flop the next state is always equal to the D input and it is independent of the present state. Therefore D must be 0 if Qn+1 has to 0,and if Qn+1 has to be 1 regardless the value of Qn.

24. Explain the flip-flop excitation tables for T flip-flop

When input T=1 the state of the flip-flop is complemented; when T=0,the state of the flip-flop remains unchanged. Therefore, for 0_0 and 1_1 transitions T must be 0 and for 0_1 and 1_0 transitions must be 1.

25. Define sequential circuit?

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

26. Give the comparison between combinational circuits and sequential circuits.

Combinational circuits Sequential circuits memory unit is not required Memory unity is required Parallel adder is a combinational circuit Serial adder is a sequential circuit

27. What do you mean by present state?

The information stored in the memory elements at any given time defines the present state of the sequential circuit.

28. What do you mean by next state?

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

29. State the types of sequential circuits?

1. Synchronous sequential circuits
2. Asynchronous sequential circuits

30. Define synchronous sequential circuit

In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time.

31. Define Asynchronous sequential circuit?

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.

32. Give the comparison between synchronous & Asynchronous sequential circuits?

Synchronous sequential circuits Asynchronous sequential circuits. Memory elements are clocked flip-flops Memory elements are either unlocked flip-flops or time delay elements. Easier to design more difficult to design

33. Define flip-flop

Flip - flop is a sequential device that normally samples its inputs and changes its outputs only at times determined by clocking signal.

34. What is race around condition?

In the JK latch, the output is feedback to the input, and therefore changes in the output results

change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

35. What are the types of shift register?

- Serial in serial out shift register
- Serial in parallel out shift register
- Parallel in serial out shift register
- Parallel in parallel out shift register
- Bidirectional shift register shift register

36. State the types of counter?

- Synchronous counter
- Asynchronous Counter

37. Give the comparison between synchronous & Asynchronous counters.

Asynchronous counters	Synchronous counters
1. In this type of counter flip-flops are connected in such a way that output of 1st flip-flop drives the clock for the next flip-flop	In this type there is no connection between output of first flip-flop and clock input of the next flip - flop
2. All the flip-flops are Not clocked simultaneously	All the flip-flops are clocked Simultaneously

UNIT IV -MEMORY DEVICES

1. Explain ROM

A read only memory(ROM) is a device that includes both the decoder and the OR gates within a single IC package. It consists of n input lines and m output lines. Each bit combination of the input variables is called an address. Each bit combination that comes out of the output lines is called a word. The number of distinct addresses possible with n input variables is 2n.

2. What are the types of ROM?

1. PROM
2. EPROM
3. EEPROM

3. Explain PROM.

PROM (Programmable Read Only Memory)

It allows user to store data or program. PROMs use the fuses with material like nichrome and polycrystalline. The user can blow these fuses by passing around 20 to 50 mA of current for the period 5 to 20μs.The blowing of fuses is called programming of ROM. The PROMs are one time programmable. Once programmed, the information is stored permanent.

4. Explain EPROM.

EPROM(Erasable Programmable Read Only Memory)

EPROM use MOS circuitry. They store 1's and 0's as a packet of charge in a buried layer of the IC chip. We can erase the stored data in the EPROMs by exposing the chip to ultraviolet light via its quartz window for 15 to 20 minutes. It is not possible to erase selective information. The chip can be reprogrammed.

5. Explain EEPROM.

EEPROM (Electrically Erasable Programmable Read Only Memory)

EEPROM also use MOS circuitry. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals.

6. What is RAM?

Random Access Memory. Read and write operations can be carried out.

7. Define ROM

A read only memory is a device that includes both the decoder and the OR gates within a single IC package.

8. Define address and word:

In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

9. What are the types of ROM.

- Masked ROM.
- Programmable Read only Memory
- Erasable Programmable Read only memory.
- Electrically Erasable Programmable Read only Memory.

10. What is programmable logic array? How it differs from ROM?

In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generates all the minterms as in the ROM.

11. What is mask - programmable?

With a mask programmable PLA, the user must submit a PLA program table to the manufacturer.

12. What is field programmable logic array?

The second type of PLA is called a field programmable logic array. The user by means of

certain recommended procedures can program the EPLA.

13. List the major differences between PLA and PAL

PLA: Both AND and OR arrays are programmable and Complex Costlier than PAL AND arrays are programmable OR arrays are fixed Cheaper and Simpler

14. Define PLD.

Programmable Logic Devices consist of a large array of AND gates and OR gates that can be programmed to achieve specific logic functions.

15. Give the classification of PLDs.

PLDs are classified as PROM(Programmable Read Only Memory), Programmable Logic Array (PLA), Programmable Array Logic (PAL), and Generic Array Logic(GAL)

16. Define PROM.

PROM is Programmable Read Only Memory. It consists of a set of fixed AND gates connected to a decoder and a programmable OR array.

17. Define PLA.

PLA is Programmable Logic Array (PLA). The PLA is a PLD that consists of a Programmable AND array and a programmable OR array.

18. Define PAL.

PAL is Programmable Array Logic. PAL consists of a programmable AND array and a fixed OR array with output logic.

19. Why was PAL developed?

It is a PLD that was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.

20. Define GAL.

GAL is Generic Array Logic. GAL consists of a programmable AND array and a fixed OR array with output logic.

21. Why the input variables to a PAL are buffered

The input variables to a PAL are buffered to prevent loading by the large number of AND gate inputs to which available or its complement can be connected.

22. What does PAL 10L8 specify?

PAL - Programmable Logic Array
10- Ten inputs
L - Active LOW Ouput
8 - Eight Outputs

23. What is CPLD?

CPLDs are Complex Programmable Logic Devices. They are larger versions of PLDs with a centralized internal interconnect matrix used to connect the device macro cells together.

24. Define bit, byte and word.

The smallest unit of binary data is bit. Data are handled in a 8 bit unit called byte. A complete unit of information is called a word which consists of one or more bytes.

25. How many words can a 16x8 memory can store?

A 16x8 memory can store 16,384 words of eight bits each

26. Define address of a memory.

The location of a unit of data in a memory is called address.

27. What is Read and Write operation?

The Write operation stores data into a specified address into the memory and the Read operation takes data out of a specified address in the memory.

28. Why RAMs are called as Volatile?

RAMs are called as Volatile memories because RAMs lose stored data when the power is turned OFF.

29. Define ROM.

ROM is a type of memory in which data are stored permanently or semi permanently. Data can be read from a ROM, but there is no write operation.

30. Define RAM.

RAM is Random Access Memory. It is a random access read/write memory. The data can be read or written into from any selected address in any sequence.

31. List the two categories of RAMs.

The two categories of RAMs are static RAM(SRAM) and dynamic RAM (DRAM).

32. Define Static RAM and dynamic RAM.

Static RAM uses flip flops as storage elements and therefore store data indefinitely as long as dc power is applied.

Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.

33. List the two types of SRAM.

Asynchronous SRAMs and Synchronous Burst SRAMs

UNIT V - SYNCHRONOUS AND AYNCHRONOUS SEQUENTIAL CIRCUITS

1. What are secondary variables?

Present state variables in asynchronous sequential circuits

2. What are excitation variables?

Next state variables in asynchronous sequential circuits

3. What is fundamental mode sequential circuit?

Input variables changes if the circuit is stable -inputs are levels, not pulsesonly one input can change at a given time

4. What is pulse mode circuit?

inputs are pulses width of pulses are long for circuit to respond to the input pulse width must not be so long that it is still present after the new state is reached

5. What are the significance of state assignment?

In synchronous circuits-state assignments are made with the objective of circuit Reduction

Asynchronous circuits-its objective is to avoid critical races

6. When does race condition occur?

Two or more binary state variables change their value in response to the change in i/p Variable

7. What is non critical race?

Final stable state does not depend on the order in which the state variable changes race condition is not harmful

8. What is critical race?

Final stable state depends on the order in which the state variable changes -race condition is harmful

9. When does a cycle occur?

Asynchronous circuit makes a transition through a series of unstable state

10. What are the steps for the design of asynchronous sequential circuit?

- construction of primitive flow table -reduction of flow table
- state assignment is made -realization of primitive flow table

11. What is hazard?

Unwanted switching transients is known as Hazards

12. What is static 1 and Static 0 hazard?

Output goes momentarily 0 when it should remain at 1 is known as ‘static 1 hazard’ and output goes momentarily 1 when it should remain at 0 is known as ‘static 0 hazard’.

13. What is dynamic hazard?

Output changes 3 or more times when it changes from 1 to 0 or 0 to 1

14. What is the cause for essential hazards?

Unequal delays along 2 or more path from same input

15. What is flow table?

State table of an synchronous sequential network

16. What is SM chart?

It describes the behavior of a state machine -used in hardware design of digital systems

17. What are the advantages of SM chart?

- Easy to understand the operation
- East to convert to several equivalent forms

18. What is primitive flow chart?

One stable state per row is called as primitive flow table.

19. What is combinational circuit?

Output depends on the given input. It has no storage element.

20. What is state equivalence theorem?

Two states SA and SB, are equivalent if and only if for every possible input X sequence, the outputs are the same and the next states are equivalent
i.e., if SA (t + 1) = SB (t + 1) and ZA = ZB then SA = SB.

21. Define compatibility.

States S_i and S_j said to be compatible states, if and only if for every input sequence that affects the two states, the same output sequence, occurs whenever both outputs are specified and regardless of whether S_i or S_j is the initial state.

22. Define merger graph.

The merger graph is defined as follows. It contains the same number of vertices as the state table contains states. A line drawn between the two state vertices indicates each compatible state pair. It two states are incompatible no connecting line is drawn.

23. Define incompatibility

The states are said to be incompatible if no line is drawn in between them. If implied states are incompatible, they are crossed & the corresponding line is ignored

24. Define state table.

For the design of sequential counters we have to relate present states and next states. The table, which represents the relationship between present states and next states, is called state table.

25. Define total state.

The combination of level signals that appear at the inputs and the outputs of the delays define what is called the total state of the circuit.

26. What are the steps for the design of asynchronous sequential circuit?

1.Construction of a primitive flow table from the problem statement.
2.Primitive flow table is reduced by eliminating redundant states using the state reduction
3.State assignment is made
4.The primitive flow table is realized using appropriate logic elements.

27. Define primitive flow table:

It is defined as a flow table which has exactly one stable state for each row in the table. The design process begins with the construction of primitive flow table.

28. What are the types of asynchronous circuits?

1. Fundamental mode circuits
2. Pulse mode circuits

29. Give the comparison between state Assignment Synchronous circuit and state assignment

- In synchronous circuit, the state assignments are made with the objective of circuit reduction.
- In asynchronous circuits, the objective of state assignment is to avoid critical races.

30. What are races?

When 2 or more binary state variables change their value in response to a change in an input

variable, race condition occurs in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.

31. Define non critical race.

If the final stable state that the circuit reaches does not depend on the order in which the state variable changes, the race condition is not harmful and it is called a non critical race.

32. Define critical race?

If the final stable state depends on the order in which the state variable changes, the race condition is harmful and it is called a critical race.

33. What is a cycle?

A cycle occurs when an asynchronous circuit makes a transition through a series of unstable states. If a cycle does not contain a stable state, the circuit will go from one unstable to stable to another, until the inputs are changed.

34. List the different techniques used for state assignment.

1. Shared row state assignment
2. One hot state assignment.

35. Write a short note on fundamental mode asynchronous circuit.

Fundamental mode circuit assumes that. The input variables change only when the circuit is stable. Only one input variable can change at a given time and inputs are levels and not pulses.

36. Write a short note on pulse mode circuit.

Pulse mode circuit assumes that the input variables are pulses instead of level. The width of the pulses is long enough for the circuit to respond to the input and the pulse width must not be so long that it is still present after the new state is reached.

37. Define secondary variables.

The delay elements provide a short term memory for the sequential circuit. The present state and next state variables in asynchronous sequential circuits are called secondary variables.

38. Define flow table in asynchronous sequential circuit.

In asynchronous sequential circuit state table is known as flow table because of the behavior of the asynchronous sequential circuit. The stage changes occur in independent of a clock, based on the logic propagation delay, and cause the states to flow from one to another.

39. What is pulse mode asynchronous machine?

A pulse mode asynchronous machine has two inputs. If produces an output whenever two consecutive pulses occur on one input line only. The output remains at 1 until a pulse has occurred on the other input line. Write down the state table for the machine.

40. What is fundamental mode?

A transition from one stable state to another occurs only in response to a change in the input state. After a change in one input has occurred, no other change in any input occurs until the circuit enters a stable state. Such a mode of operation is referred to as a fundamental mode.