MULTIPLE CHOICE QUESTIONS ON EMBEDDED SYSTEMS

1. Which of the following is a coprocessor of 80386?
a) 80387
b) 8087
c) 8089
d) 8088
View Answer

Answer: a
Explanation: 80386 have 80387 as a floating point arithmetic coprocessor which can perform various floating point calculations.

2. Name the processor which helps in floating point calculations.
a) microprocessor
b) microcontroller
c) coprocessor
d) controller
View Answer

Answer: c
Explanation: The coprocessor can perform signal processing, floating point arithmetics, encryption etc.

3. Which is the coprocessor of 8086?
a) 8087
b) 8088
c) 8086
d) 8080
View Answer

Answer: a
Explanation: 8087 is the coprocessor for both 8086 and 8088. 8089 is also a coprocessor of 8086 and 80888.

4. Which of the following is a coprocessor of Motorola 68000 family?
a) 68001
b) 68011
c) 68881
d) 68010
View Answer

Answer: c
Explanation: The 68881 coprocessor of Motorola provides floating point arithmetics.

5. Which of the following processors can perform exponential, logarithmic and trigonometric functions?
a) 8086
b) 8087
c) 8080
d) 8088
View Answer

Answer: b
Explanation: 8087 is a coprocessor which can perform all the mathematical functions including addition, subtraction, multiplication, division, exponential, logarithmic, trigonometric etc. 8086, 8080 and 8088 are microprocessors which require the help of a coprocessor for floating point arithmetic.

6. How many stack register does an 8087 have?
a) 4
b) 8
c) 16
d) 32
View Answer

Answer: b
Explanation: The 8087 coprocessor does not have a main register set but they have an 8-level deep stack register from st0 to st7.

7. Which of the following processor can handle infinity values?
a) 8080
b) 8086
c) 8087
d) 8088
View Answer

Answer: c
Explanation: 8087 is a coprocessor which can handle infinity values with two types of closure known as affine closure and projective closure.

8. Which coprocessor supports affine closure?
a) 80187
b) 80287
c) 80387
d) 8088
View Answer

Answer: b
Explanation: 80287 uses an affine closure for infinity values whereas 80387 and 80187 support projective closure for infinity values.

9. Which one is the floating point coprocessor of 80286?
a) 8087
b) 80187
c) 80287
d) 80387
View Answer

Answer: c
Explanation: 80286 supports 80287 as its floating point coprocessor which helps in floating point calculations.

10. How many pins does 8087 have?
a) 40 pin DIP
b) 20 pin DIP
c) 40 pins
d) 20 pins
View Answer

Answer: a
Explanation: All 8087 models have a 40 pin DIP which is operated in 5V.

11. What is the clock frequency of 8087?
a) 10 MHz
b) 5 MHz
c) 6 MHz
d) 4 MHz
View Answer

12. How are negative numbers stored in a coprocessor?
a) 1’s complement
b) 2’s complement
c) decimal
d) gray
View Answer

Answer: b
Explanation: In a coprocessor, negative numbers are stored in 2’s complement with its leftmost sign bit of 1 whereas positive numbers are stored in the form of true value with its leftmost sign bit of 0.

13. How many bits are used for storing signed integers?
a) 2
b) 4
c) 8
d) 16
View Answer

Answer: d
Explanation: Signed integers in a coprocessor are stored as 16-bit word, 32-bit double word or 64-bit quadword.

14. Which of the processor has an internal coprocessor?
a) 8087
b) 80287
c) 80387
d) 80486DX
View Answer

Answer: d
Explanation: 8087 is an external IC designed to operate with the 8088/8086 processor but 80486DX is an on-chip coprocessor that is, it does not require an extra integrated chip for floating point arithmetics.

15. What are the two major sections in a coprocessor?
a) control unit and numeric control unit
b) integer unit and control unit
c) floating point unit and coprocessor unit
d) coprocessor unit and numeric control unit
View Answer

Answer: a
Explanation: Control unit interfaces the coprocessor with its main microprocessor whereas numeric control unit can execute the coprocessor instructions

15. Which are the processors based on RISC?
a) SPARC
b) 80386
c) MC68030
d) MC68020
View Answer

Answer: a
Explanation: SPARC and MIPS processors are the first generation processors of RISC architecture.

16. What is 80/20 rule?
a) 80% instruction is generated and 20% instruction is executed
b) 80% instruction is executed and 20% instruction is generated
c) 80%instruction is executed and 20% instruction is not executed
d) 80% instruction is generated and 20% instructions are not generated
View Answer

Answer: a
Explanation: 80% of instructions are generated and only 20% of the instruction set is executed that is, by simplifying the instructions, the performance of the processor can be increased which lead to the formation of RISC that is reduced instruction set computing.

17. Which of the architecture is more complex?
a) SPARC
b) MC68030
c) MC68030
d) 8086
View Answer

Answer: a
Explanation: SPARC have RISC architecture which has a simple instruction set but MC68020, MC68030, 8086 have CISC architecture which is more complex than CISC.

18. Which is the first company who defined RISC architecture?
a) Intel
b) IBM
c) Motorola
d) MIPS
View Answer

Answer: b
Explanation: In 1970s IBM identified RISC architecture.

19. Which of the following processors execute its instruction in a single cycle?
a) 8086
b) 8088
c) 8087
d) MIPS R2000
View Answer

Answer: d
Explanation: MIPS R2000 possess RISC architecture in which the processor executes its instruction in a single clock cycle and also synthesize complex operations from the same reduced instruction set.

20. How is memory accessed in RISC architecture?
a) load and store instruction
b) opcode instruction
c) memory instruction
d) bus instruction
View Answer

Answer: a
Explanation: The data of memory address is loaded into a register and manipulated, its contents are written out to the main memory.

21. Which of the following has a Harvard architecture?
a) EDSAC
b) SSEM
c) PIC
d) CSIRAC
View Answer

Answer: c
Explanation: PIC follows Harvard architecture in which the external bus architecture consist of separate buses for instruction and data whereas SSEM, EDSAC, CSIRAC are stored program architecture.

22. Which of the following statements are true for von Neumann architecture?
a) shared bus between the program memory and data memory
b) separate bus between the program memory and data memory
c) external bus for program memory and data memory
d) external bus for data memory only
View Answer

Answer: a
Explanation: von Neumann architecture shares bus between program memory and data memory whereas Harvard architecture have a separate bus for program memory and data memory.

23. What is CAM stands for?
a) content-addressable memory
b) complex addressable memory
c) computing addressable memory
d) concurrently addressable memory
View Answer

Answer: a
Explanation: Non-von Neumann architecture is based on content-addressable memory.

24. Which of the following processors uses Harvard architecture?
a) TEXAS TMS320
b) 80386
c) 80286
d) 8086
View Answer

Answer: a
Explanation: It is a digital signal processor which have small and highly optimized audio or video processing signals. It possesses multiple parallel data bus.

25. Which company further developed the study of RISC architecture?
a) Intel
b) Motorola
c) university of Berkeley
d) MIPS
View Answer

Answer: c
Explanation: The University of Berkeley and Stanford university provides the basic architecture model of RISC.

26. Princeton architecture is also known as
a) von Neumann architecture
b) Harvard
c) RISC
d) CISC
View Answer

Answer: a
Explanation: The von Neumann architecture is also known as von Neumann model or Princeton architecture.

27. Who coined the term RISC?
a) David Patterson
b) von Neumann
c) Michael J Flynn
d) Harvard
View Answer

Answer: a
Explanation: David Patterson of Berkeley university coined the term RISC whereas Michael J Flynn who first views RISC.

28. Which of the following is an 8-bit RISC Harvard architecture?
a) AVR
b) Zilog80
c) 8051
d) Motorola 6800
View Answer

Answer: a
Explanation: AVR is an 8-bit RISC architecture developed by Atmel. Zilog80, 8051, Motorola 6800 are having CISC architectures.

29. Which of the following processors has CISC architecture?
a) AVR
b) Atmel
c) Blackfin
d) Zilog Z80
View Answer

Answer: d
Explanation: Zilog80 have CISC architecture whereas AVR, Atmel and blackfin possess RISC architecture

30. Which is the most basic non-volatile memory?
a) Flash memory
b) PROM
c) EPROM
d) ROM
View Answer

Answer: d
Explanation: The basic non-volatile memory is ROM or mask ROM, and the content of ROM is fixed in the chip which is useful in firmware programs for booting up the system.

31. Who has invented flash memory?
a) Dr.FujioMasuoka
b) John Ellis
c) Josh Fisher
d) John Ruttenberg
View Answer

Answer: a
Explanation: Flash memory is invented by Dr. FujioMasuoka at Toshiba in the 1980s which are a non-volatile memory.

32. Which of the following is serial access memory?
a) RAM
b) Flash memory
c) Shifters
d) ROM
View Answer

Answer: c
Explanation: The memory arrays are basically divided into three which are random access memory, serial access memory, and content address memory. Serial access memory is divided into two, theses are shifters and queues.

33. Which is the early form of non-volatile memory?
a) magnetic core memory
b) ferrimagnetic memory
c) anti-magnetic memory
d) anti-ferromagnetic
View Answer

Answer: a
Explanation: The early form of non-volatile memory is known as magnetic core memory in which the ferromagnetic ring was magnetised to store data.

34. Which of the following memories has more speed in accessing data?
a) SRAM
b) DRAM
c) EPROM
d) EEPROM
View Answer

Answer: a
Explanation: SRAM have more speed than DRAM because it has 4 to 6 transistors arranged as flip-flop logic gates, that is it can be flipped from one binary state to another but DRAM has a small capacitor as its storage element.

35. In which memory, the signals are multiplexed?
a) DRAM
b) SRAM
c) EPROM
d) EEPROM
View Answer

Answer: a
Explanation: The signals in address bus are multiplexed with DRAM non-multiplexed with SRAM.

36. How many main signals are used with memory chips?
a) 2
b) 4
c) 6
d) 8
View Answer

Answer: b
Explanation: The main signals associated with memory chips are four. These are the signals associated with address bus, data bus, chip select signals, and control signals for read and write operations.

37. What is the purpose of address bus?
a) to provide data to and from the chip
b) to select a specified chip
c) to select a location within the memory chip
d) to select a read/write cycle
View Answer

Answer: c
Explanation: Address bus is used to choose a particular location in the memory chip. Data bus is used to provide data to and from the chip. Chip select signals are used to select a particular chip within the memory.

38. Which are the two main types of processor connection to the motherboard?
a) sockets and slots
b) sockets and pins
c) slots and pins
d) pins and ports
View Answer

Answer: a
Explanation: The type of processor which connects to a socket on the bottom surface of the chip that connects to the motherboard by Zero Insertion Force Socket. Intel 486 is an example of this type of connection. The processor slot is one which is soldered into a card, which connects to a motherboard by a slot. Example for slot connection is Pentium 3.

39. Which of the following has programmable hardware?
a) microcontroller
b) microprocessor
c) coprocessor
d) FPGA
View Answer

Answer: d
Explanation: Field programmable gate arrays is a type of multi-core architecture whose hardware function can be programmed by using hardware design tools.

40. Who invented TriMedia processor?
a) Intel
b) IBM
c) Apple
d) NXP Semiconductor
View Answer

Answer: d
Explanation: TriMedia is a VLIW processor from NXP Semiconductor in Netherlands. It possesses a Harvard architecture CPU for video and audio applications

41. Which of the following have a 16 Mbytes addressed range?
a) PowerPC
b) M68000
c) DSP56000
d) TMS 320
View Answer

Answer: b
Explanation: The M68000 family has a 16 Mbyte addressing range. The PowerPC family has a larger 4 Gbyte range and the DSP56000 has a 128-kilo word address space.

42. Which of the following can destroy the accuracy in the algorithms?
a) delays
b) error signal
c) interrupt
d) mmu
View Answer

Answer: a
Explanation: The delays occurring in the memory management unit can destroy the accuracy in the algorithms and in order to avoid this, the linear addressing range should be increased.

43. How many numbers of ways are possible for allocating the memory to the modular blocks?
a) 1
b) 2
c) 3
d) 4
View Answer

Answer: c
Explanation: Most of the systems have a multitasking operating system in which the software consist of modular blocks of codes which run under the control of the operating system. There are three ways for allocating memory to these blocks. The first way distributes the block in a predefined way. The second way for allocating memory includes relocation or position independency in the software and the other way of allocating memory to the block is the address translation in which the logical address is translated to the physical address.

44. Which of the following is replaced with the absolute addressing mode?
a) relative addressing mode
b) protective addressing mode
c) virtual addressing mode
d) temporary addressing mode
View Answer

Answer: a
Explanation: The memory allocation of the modular blocks can be done by the writing the software program in relocatable or position independent manner which can execute anywhere in the memory map, but relocatable code must have the same address between its data and code segments. This is used to avoid the use of absolute addressing modes which is replaced by the relative addressing modes.

45. What is the main purpose of the memory management unit?
a) address translation
b) large storage
c) reduce the size
d) provides address space
View Answer

Answer: a
Explanation: The memory management unit handles with physical addresses. Therefore, the virtual or the logical address is first translated to the physical address.

46. Which of the following provides stability to the multitasking system?
a) memory
b) DRAM
c) SRAM
d) Memory partitioning
View Answer

Answer: d
Explanation: The memory partitioning provides stability to the multitasking system so that the errors within one task will not corrupt the other tasks.

47. Which of the following is used by the M68000 family?
a) M68000
b) 80386
c) 8086
d) 80286
View Answer

Answer: a
Explanation: The M68000 uses memory partitioning by the use of function code or by the combination of superscalar signals and the Harvard architecture.

48. What can be done for the fine grain protection of the processor?
a) add extra description bit
b) add error signal
c) add wait stage
d) remains unchanged
View Answer

Answer: a
Explanation: The finer grain protection of memory management is achieved by the addition of extra description bit to an address to declare its status. The memory management unit can detect an error if the task attempts to access memory that has not been allocated to it or a certain kind of mismatch occurs.

49. Which of the following technique is used by the UNIX operating system?
a) logical address memory
b) physical address memory
c) virtual memory technique
d) translational address
View Answer

Answer: c
Explanation: In the workstation and in the UNIX operating system virtual memory technique is frequently used in which the main memory is divided into different segments and pages. These pages will have a virtual address which can increase the address spacing.

50. Which of the following consist two lines of legs on both sides of a plastic or ceramic body?
a) SIMM
b) DIMM
c) Zig-zag
d) Dual in-line
View Answer

Answer: d
Explanation: The dual-in-line package consists of two lines of legs on both sides of the plastic or ceramic. Most commonly used is BIOS EPROMs, DRAM and SRAM.

51. Which of the following can transfer multiple bits of data simultaneously?
a) serial port
b) sequential port
c) concurrent unit
d) parallel port
View Answer

Answer: d
Explanation: The parallel port can transfer multiple bits of data simultaneously. It provides the input or output binary data with a single bit allocated to each pin within the port.

52. Which of the following are interfaced as inputs to the parallel ports?
a) LEDs
b) switch
c) alphanumeric display
d) seven segmented display
View Answer

Answer: b
Explanation: The LEDs, alphanumeric displays, seven segment displays are interfaced for the output whereas the switch is an input port.

53. Which of the following are interfaced as the outputs to the parallel ports?
a) keyboards
b) switches
c) LEDs
d) knobs
View Answer

Answer: c
Explanation: The keyboards, switches, and knobs are used as output whereas the LEDs are used as the input port.

54. How many registers are there to control the parallel port in the basic form?
a) 1
b) 3
c) 2
d) 5
View Answer

Answer: c
Explanation: The basic operation of the parallel port dealt with two types of registers which are called data direction register and the data register.

55. Which of the following is also known as tri-state?
a) output port
b) input port
c) parallel port
d) output-input port
View Answer

Answer: a
Explanation: The progression in the parallel ports provides a third register or an individual control bit which can make the pin in a high impedance state. An output port which can do this is also known as tri-state, that is, logic high, logic low and a high impedance state.

56. How buffers are enabled in the parallel ports?
a) by the data register
b) by data direction register
c) by individual control register
d) by data and individual control register
View Answer

Answer: b
Explanation: The implementation of parallel port uses a couple of buffers which are enabled by the data direction register by setting the corresponding bit of the register.

57. Which of the following registers offers high impedance?
a) data register
b) data direction register
c) individual control bit
d) data register and data direction register
View Answer

Answer: c
Explanation: The register which offers high impedance is the individual control bit or the third register which can be implemented by switching off both the buffers and putting their connections to the pin which offers high impedance.

58. Which of the following can be used as a chip select?
a) multifunction I/O port
b) parallel port
c) DMA port
d) memory port
View Answer

Answer: a
Explanation: The multifunction I/O port can also be used a chip select for the memory design. The function that the pin performs is set up internally through the use of a function register which internally configures how the external pins are connected internally.

59. Which of the following is necessary for the parallel input-output port?
a) inductor
b) pull-up resistor
c) push-up resistor
d) capacitor
View Answer

Answer: b
Explanation: The I/O port needs an external pull-up resistor. In some devices, it offers internally. If it is not provided, it can cause incorrect data on reading the port and it prevents the port from turning off an external device.

60. Which of the following can be described as general-purpose?
a) multifunction I/O port
b) input port
c) DMA port
d) output port
View Answer

Answer: a
Explanation: The multifunction I/O ports can be described as the general-purpose and it can be shared with other peripherals

61. What does UART stand for?
a) universal asynchronous receiver transmitter
b) unique asynchronous receiver transmitter
c) universal address receiver transmitter
d) unique address receiver transmitter
View Answer

Answer: a
Explanation: The UART or universal asynchronous receiver transmitter is used for the data transmission at a predefined speed or baud rate.

62. How is data detected in a UART?
a) counter
b) timer
c) clock
d) first bit
View Answer

Answer: c
Explanation: The data can be detected by the local clock reference which is generated from the baud rate generator.

63. Which of the signal is set to one, if no data is transmitted?
a) READY
b) START
c) STOP
d) TXD
View Answer

Answer: d
Explanation: The TXD signal goes to logic one, when no data is transmitted. When data transmits, it sets to logic zero.

64. What rate can define the timing in the UART?
a) bit rate
b) baud rate
c) speed rate
d) voltage rate
View Answer

Answer: b
Explanation: The timing is defined by the baud rate in which both the transmitter and receiver are used. The baud rate is supplied by the counter or an external timer called baud rate generator which generate a clock signal.

65. How is baud rate supplied?
a) baud rate voltage
b) external timer
c) peripheral
d) internal timer
View Answer

Answer: b
Explanation: The baud rate is supplied by the counter or an external timer called baud rate generator which generate a clock signal.

66. Which is the most commonly used UART?
a) 8253
b) 8254
c) 8259
d) 8250
View Answer

Answer: d
Explanation: The Intel 8253, 8254 and 8259 are timers whereas Intel 8250 is a UART which is commonly used.

67. Which company developed 16450?
a) Philips
b) Intel
c) National semiconductor
d) IBM
View Answer

Answer: c
Explanation: The Intel 8250 is replaced by the 16450 and 16550 which are developed by the National Semiconductors. 16450 is a chip which can combines all the PC's input output devices into a single piece of silicon.

68. What does ADS indicate in 8250 UART?
a) address signal
b) address terminal signal
c) address strobe signal
d) address generating signal
View Answer

Answer: b
Explanation: The ADS is address strobe signal and is working as active low in 8250 UART. The ADS signal is used to latch the address and chip select signals while a processor access.

69. Which of the following signals are active low in the 8250 UART?
a) BAUDOUT
b) DDIS
c) INTR
d) MR
View Answer

Answer: a
Explanation: The BAUDOUT signal is active low whereas DDIS, INTR and MR are active high in the 8250 UART. BAUDOUT is the clock signal from the transmitter part of the UART. DDIS signal goes low when the CPU is reading data from the UART. INTR is the interrupt pin. MR is the master reset pin.

70. Which of the signal can control bus arbitration logic in 8250?
a) MR
b) DDIS
c) INTR
d) RCLK
View Answer

Answer: b
Explanation: DDIS signal goes low when the CPU is reading data from the UART and it also controls the bus arbitration logic

71. Which of the following can be used for long distance communication?
a) I2C
b) Parallel port
c) SPI
d) RS232
View Answer

Answer: d
Explanation: A slightly different serial port called RS232 is used for long distance communication, otherwise the clock may get skewed. The low voltage signal also affect the long distance communication.

72. Which of the following can affect the long distance communication?
a) clock
b) resistor
c) inductor
d) capacitor
View Answer

Answer: a
Explanation: For small distance communication, the clock signal which allows a synchronous transmission of data is more than enough, and the low voltage signal of TTL or CMOS is sufficient for the operation. But for long distance communication, the clock signal may get skewed and the low voltage can be affected by the cable capacitance. So for long distance communication RS232 can be used.

73. Which are the serial ports of the IBM PC?
a) COM1
b) COM4 and COM1
c) COM1 and COM2
d) COM3
View Answer

Answer: c
Explanation: The IBM PC has one or two serial ports called the COM1 and the COM2, which are used for the data transmission between the PC and many other peripheral units like printer, modem etc.

74. Which of the following can provide hardware handshaking?
a) RS232
b) Parallel port
c) Counter
d) Timer
View Answer

Answer: a
Explanation: In RS232, several lines are used for transmitting and receiving data and these also provide a control for the hardware handshaking.

75. Which of the following have an asynchronous data transmission?
a) SPI
b) RS232
c) Parallel port
d) I2C
View Answer

Answer: b
Explanation: The data is transmitted asynchronously in RS232 which enhance long distance communication, whereas SPI, I2C offers short distance communication, and therefore, they are using synchronous data transmission.

76. How many areas does the serial interface have?
a) 1
b) 3
c) 2
d) 4
View Answer

Answer: c
Explanation: The serial interface is divided into two, physical interface and the electrical interface.

77. The RS232 is also known as
a) UART
b) SPI
c) Physical interface
d) Electrical interface
View Answer

Answer: d
Explanation: The RS232 is also known as the physical interface and it is also known as EIA232.

78. How much voltage does the MC1489 can take ?
a) 12V
b) 5V
c) 3.3V
d) 2.2V
View Answer

Answer: b
Explanation: The MC1489 is a interface chip which can take a 5V and generate internally the other voltages which are needed to meet the interface specification.

79. Which of the following is not a serial protocol?
a) SPI
b) I2C
c) Serial port
d) RS232
View Answer

Answer: d
Explanation: The RS232 is a physical interface. It does not follow the serial protocol.

80. Which of the following is an ideal interface for LCD controllers?
a) SPI
b) parallel port
c) Serial port
d) M-Bus
View Answer

Answer: d
Explanation: M-Bus or Motorola Bus is an ideal interface for LCD controllers, A/D converters, EEPROMs and many other components which can benefit faster transmission.

81. Which of the following works by dividing the processor's time?
a) single task operating system
b) multitask operating system
c) kernel
d) applications
View Answer

Answer: b
Explanation: The multitasking operating system works by dividing the processor's time into different discrete time slots, that is, each application requires a defined number of time slots to complete its execution.

82. Which of the following decides which task can have the next time slot?
a) single task operating system
b) applications
c) kernel
d) software
View Answer

Answer: c
Explanation: The operating system kernel decides which task can have the next time slot. So instead of the task executing continuously until completion, the execution of the processor is interleaved with the other tasks.

83. Which of the following controls the time slicing mechanism in a multitasking operating system?
a) kernel
b) single tasking kernel
c) multitasking kernel
d) application manager
View Answer

Answer: c
Explanation: The multitasking operating systems are associated with the multitasking kernel which controls the time slicing mechanism.

84. Which of the following provides time period for the context switch?
a) timer
b) counter
c) time slice
d) time machine
View Answer

Answer: c
Explanation: The time period required for each task for execution before it is stopped and replaced during a context switch is known as the time slice.

85. Which of the following can periodically trigger the context switch?
a) software interrupt
b) hardware interrupt
c) peripheral
d) memory
View Answer

Answer: b
Explanation: The time period required for each task for execution before it is stopped and replaced during a context switch is known as the time slice. These are periodically triggered by a hardware interrupt from the system timer.

86. Which interrupt provides system clock in the context switching?
a) software interrupt
b) hardware interrupt
c) peripheral
d) memory
View Answer

Answer: b
Explanation: The multitasking operating systems deals with the multitasking kernel which controls the time slicing mechanism and the time period required for each task for execution before it is stopped and replaced during a context switch is known as the time slice which are periodically triggered by a hardware interrupt from the system timer. This hardware interrupt provides the system clock in which several interrupts are executed and counted before a context switch is performed.

87. The special tale in the multitasking operating system is also known as
a) task control block
b) task access block
c) task address block
d) task allocating block
View Answer

Answer: a
Explanation: When a context switch is performed, the current program or task is interrupted, so the processor's registers are saved in a special table which is known as task control block.

88. Which of the following stores all the task information that the system requires?
a) task access block
b) register
c) accumulator
d) task control block
View Answer

Answer: d
Explanation: The task control block stores all the task information that the system requires and this is done when the context switch is performed so that the currently running program is interrupted.

89. Which of the following contains all the task and their status?
a) register
b) ready list
c) access list
d) task list
View Answer

Answer: b
Explanation: The ‘ready’ list possesses all the information regarding a task, that is, all the task and its corresponding status which is used by the scheduler to decide which task should execute in the next time slice.

90. Which determines the sequence and the associated task’s priority?
a) scheduling algorithm
b) ready list
c) task control block
d) application register
View Answer

Answer: a
Explanation: The scheduling algorithm determines the sequence and an associated task’s priority. It also determines the present status of the task

91. Which of the following can be used to refer to entities within the RTOS?
a) threads
b) kernels
c) system
d) applications
View Answer

Answer: a
Explanation: The threads and processes can be used to refer to entities within the RTOS. They provide an interchangeable replacement for the task. They have a slight difference in their function.

92. Which of the following defines the set of instructions loaded into the memory?
a) process
b) task
c) thread
d) system hardware
View Answer

Answer: b
Explanation: The task can be defined by the set of instructions which is loaded into the memory and it can split into two or more tasks.

3. Which of the following uses its own address space?
a) thread
b) process
c) task
d) kernel
View Answer

Answer: a
Explanation: Threads uses a shared memory space and it uses the memory space of the process.

94. Which of the following does not uses a shared memory?
a) process
b) thread
c) task
d) kernel
View Answer

Answer: a
Explanation: The program in execution is known as the process. The process does not share the memory space but the threads have a shared memory address. When the CPU switches from process to another, the current information is stored in the process descriptor.

95. Which of the following can own and control the resources ?
a) thread
b) task
c) system
d) peripheral
View Answer

Answer: b
Explanation: The task and process have several characteristics and one such is that the task or process can own or control resources and it has threads of execution which are the paths through the code.

96. Which can be supported if the task or process maintains a separate data area for each thread?
a) single thread system
b) mono thread system
c) multiple threads
d) dual threads
View Answer

Answer: c
Explanation: The multiple threads can be supported only if the process or task can maintain a separate data areas for each thread.

97. Which of the following possesses threads of execution?
a) process
b) thread
c) kernel
d) operating system
View Answer

Answer: a
Explanation: The process has threads of execution which are the paths through the code.

98. Which of the following is inherited from the parent task?
a) task
b) process
c) thread
d) kernel
View Answer

Answer: c
Explanation: The threads are a part of the process, that is, it uses a shared memory of the process and therefore said that its resources are inherited from the parent process or task.

99. Which term is used to encompass more than a simple context switch?
a) process
b) single thread system
c) thread
d) multithread
View Answer

Answer: a
Explanation: The process includes the additional information which is used to encompass more than a simple context switch. This is similar to the task switching, that is why it is said that process and task are interchangeable.

100. Which can be considered as the lower level in the multitasking operating system?
a) process
b) task
c) threads
d) multi threads
View Answer

Answer: c
Explanation: In the multitasking operating system, the process and tasks form the higher level whereas the thread is the lower level. But in a simple operating system, there is no difference between the context switch of thread and the process

101. Which of the following are the pin efficient method of communicating between other devices?
a) serial port
b) parallel port
c) peripheral port
d) memory port
View Answer

Answer: a
Explanation: The serial ports are considered to be the pin efficient method of communication between other devices within an embedded system.

102. Which of the following depends the number of bits that are transferred?
a) wait statement
b) ready statement
c) time
d) counter
View Answer

Answer: c
Explanation: The time taken for the data transmission within the system depends on the clock frequency and the number of bits that are transferred.

103. Which of the following is the most commonly used buffer in the serial porting?
a) LIFO
b) FIFO
c) FILO
d) LILO
View Answer

Answer: b
Explanation: Most of the serial ports uses a FIFO buffer so that the data is not lost. The FIFO buffer is read to receive the data, that is, first in first out.

104. What does SPI stand for?
a) serial parallel interface
b) serial peripheral interface
c) sequential peripheral interface
d) sequential port interface
View Answer

Answer: b
Explanation: The serial parallel interface bus is a commonly used interface which involves master slave mechanism. The shift registers are worked as master and the slave devices are driven by a common clock.

105. Which allows the full duplex synchronous communication between the master and the slave?
a) SPI
b) serial port
c) I2C
d) parallel port
View Answer

Answer: a
Explanation: The serial peripheral interface allows the full duplex synchronous communication between the master and the slave devices. MC68HC05 developed by Motorola uses SPI for interfacing the peripheral devices.

106. Which of the following processor uses SPI for interfacing?
a) 8086
b) 8253
c) 8254
d) MC68HC11
View Answer

Answer: d
Explanation: The MC68HC05 and MC68HC11 microcontrollers uses the serial peripheral interface for the peripheral interfacing.

107. In which register does the data is written in the master device?
a) index register
b) accumulator
c) SPDR
d) status register
View Answer

Answer: c
Explanation: The serial peripheral interface follows a master slave mechanism in which the data is written to the SPDR register in the master device and clocked out into the slave device SPDR by using a common clock signal called SCK.

108. What happens when 8 bits are transferred in the SPI?
a) wait statement
b) ready statement
c) interrupt
d) remains unchanged
View Answer

Answer: c
Explanation: The interrupts are locally generated when 8-bits are transferred so that the data can be read before the next byte is clocked through.

109. Which signal is used to select the slave in the serial peripheral interfacing?
a) slave select
b) master select
c) interrupt
d) clock signal
View Answer

Answer: a
Explanation: The slave select signal selects which slave is to receive data from the master.

110. How much time period is necessary for the slave to receive the interrupt and transfer the data?
a) 4 clock time period
b) 8 clock time period
c) 16 clock time period
d) 24 clock time period
View Answer

Answer: b
Explanation: The SPI uses an eight clock time period for the slave to receive the interrupt and transfer the data which determines the maximum data rate.

111. Which of the following allows a lower priority task to run despite the higher priority task is active and waiting to preempt?
a) message queue
b) message passing
c) semaphore
d) priority inversion
View Answer

Answer: d
Explanation: The priority inversion mechanism where the lower priority task can continue to run despite there being a higher priority task active and waiting to preempt.

112. What happens to the interrupts in an interrupt service routine?
a) disable interrupt
b) enable interrupts
c) remains unchanged
d) ready state
View Answer

Answer: a
Explanation: In the interrupt service routine, all the other interrupts are disabled till the routine completes which can cause a problem if another interrupt is received and held pending. This can result in priority inversion.

113. Which of the following is a part of RTOS kernel?
a) memory
b) input
c) ISR
d) register
View Answer

Answer: c
Explanation: The ISR can send the message for the tasks and it is a part of RTOS kernel.

114. Which of the following is an industrial interconnection bus?
a) bus interface unit
b) data bus
c) address bus
d) VMEbus
View Answer

Answer: d
Explanation: The VMEbus is an interconnection bus which is used in the industrial control and many other real-time applications.

115. Which of the following supports seven interrupt priority level?
a) kernel
b) operating system
c) VMEbus
d) data bus
View Answer

Answer: c
Explanation: The VMEbus supports seven interrupt priority level which allows the prioritisation of the resources

116. Which allows the parallel development of the hardware and software in the simulation?
a) high-level language simulation
b) low-level language simulation
c) cpu simulator
d) onboard simulator
View Answer

Answer: a
Explanation: The high-level language simulation allows a parallel development of the software and the hardware and when two parts are integrated, that will work. It can simulate I/O using the keyboard as the inputs or task which passes input data for other modules.

117. Which of the following are used to test the software?
a) data entity
b) data entry
c) data table
d) data book
View Answer

Answer: c
Explanation: In the high-level language simulation, many techniques are used to simulate the

system and one such is the data table which contains the data sequences which are used to test the software.

118. Which allows the UNIX software to be ported using a simple recompilation?
a) pSOS+
b) UNIX compatible library
c) pSOS+m
d) pOS+kernel
View Answer

Answer: b
Explanation: The most of the operating system supports or provide the UNIX-compatible library which supports the UNIX software to be ported using a simple recompilation.

119. Which of the following can simulate the processor, memory, and peripherals?
a) input simulator
b) peripheral simulator
c) memory simulator
d) cpu simulator
View Answer

Answer: d
Explanation: The CPU simulator can simulate the memory, processor, and the peripherals and allow the low-level assembler code and the small HLL programs to be tested without the actual hardware.

120. How many categories are there for the low-level simulation?
a) 2
b) 3
c) 4
d) 5
View Answer

Answer: a
Explanation: There are two categories for the low-level simulation. The first category simulates the memory system, programming model and can offer simple debugging tools whereas the second category simulation provides timing information based on the number of clocks.

121. Which of the following can simulate the LCD controllers and parallel ports?
a) memory simulator
b) sds
c) input simulator
d) output tools
View Answer

Answer: b
Explanation: There are certain tools which provide powerful tools for simulation and one such is the SDS which can simulate the processor, memory systems, integrated processor, onboard peripherals such as LCD controllers and parallel ports.

122. Which of the following provides a low-level method of debugging software?
a) high-level simulator
b) low-level simulator
c) onboard debugger
d) cpu simulator
View Answer

Answer: c
Explanation: The onboard debugger provides a very low-level method of simulating or debugging the software. It usually handles EPROMs which are plugged into the board or a set of application codes by providing a serial connection to communicate with the PC or workstation.

123. Which of the following has the ability to download code using a serial port?
a) cpu simulator
b) high-level language simulator
c) onboard debugger
d) low-level language simulator
View Answer

Answer: c
Explanation: The onboard debugger has the ability to download code from a floppy disk or by using a serial port.

124. What does the processor fetches from the EPROM if the board is powered?
a) reset vector
b) ready vector
c) start vector
d) acknowledge vector
View Answer

Answer: a
Explanation: The processor fetches its reset vector from the table which is stored in the EPROM when the board is powered and then starts the initialize the board.

125. Which of the following device can transfer the vector table from the EPROM?
a) ROM
b) RAM
c) CPU
d) peripheral
View Answer

Answer: b
Explanation: When the board gets powered up, the reset vector from the table stored in the EPROM makes the initialisation of the board and is transferred to the RAM from the EPROM through the hardware where the EPROM memory address is temporarily altered.

126. Which of the following allows the reuse of the software and the hardware components?
a) platform based design
b) memory design
c) peripheral design
d) input design
View Answer

Answer: a
Explanation: The platform design allows the reuse of the software and the hardware components in order to cope with the increasing complexity in the design of embedded systems.

127. Which of the following is the design in which both the hardware and software are considered during the design?
a) platform based design
b) memory based design
c) software/hardware codesign
d) peripheral design
View Answer

Answer: c
Explanation: The software/hardware codesign is the one which having both hardware and software design concerns. This will help in the right combination of the hardware and the software for the efficient product.

128. What does API stand for?
a) address programming interface
b) application programming interface
c) accessing peripheral through interface
d) address programming interface
View Answer

Answer: b
Explanation: The platform-based design helps in the reuse of both the hardware and the software components. The application programming interface helps in extending the platform towards the software applications.

129. Which activity is concerned with identifying the task at the final embedded systems?
a) high-level transformation
b) compilation
c) scheduling

d) task-level concurrency management
View Answer

Answer: d
Explanation: There are many design activities associated with the platforms in the embedded system and one such is the task-level concurrency management which helps in identifying the task that needed to be present in the final embedded systems.

130. In which design activity, the loops are interchangeable?
a) compilation
b) scheduling
c) high-level transformation
d) hardware/software partitioning
View Answer

Answer: c
Explanation: The high-level transformation are responsible for the high optimizing transformations, that is, the loops can be interchanged so that the accesses to array components become more local.

131. Which design activity helps in the transformation of the floating point arithmetic to a fixed point arithmetic?
a) high-level transformation
b) scheduling
c) compilation
d) task-level concurrency management
View Answer

Answer: a
Explanation: The high-level transformation are responsible for the high optimizing transformations, that is, for the loop interchanging and the transformation of the floating point arithmetic to the fixed point arithmetic can be done by the high-level transformation.

132. Which design activity is in charge of mapping operations to hardware?
a) scheduling
b) high-level transformation
c) hardware/software partitioning
d) compilation
View Answer

Answer: c
Explanation: The hardware/software partitioning is the activity which is in charge of mapping operations to the software or to the hardware.

133. Which of the following is approximated during hardware/software partitioning, during task-level concurrency management?
a) scheduling
b) compilation
c) task-level concurrency management
d) high-level transformation
View Answer

Answer: a
Explanation: The scheduling is performed in several contexts. It should be approximated with the other design activities like the compilation, hardware/software partitioning, and task-level concurrency management. The scheduling should be precise for the final code.

134. Which of the following is a process of analyzing the set of possible designs?
a) design space exploration
b) scheduling
c) compilation
d) hardware/software partitioning
View Answer

Answer: a
Explanation: The design space exploration is the process of analyzing the set of designs and the design which meet the specification is selected.

135. Which of the following is a meet-in-the-middle approach?
a) peripheral based design
b) platform based design
c) memory based design
d) processor design
View Answer

Answer: b
Explanation: The platform is an abstraction layer which covers many possible refinements to a lower level and is mainly follows a meet-in-the-middle approach