Integrated Circuits

1. What is the best choice of IC package used for experimental purpose?
a) DIP package
b) Metal can package
c) Flat pack
d) Transistor pack
Answer: a
Explanation: DIP package are used as it is easy to mount. The mounting does not require bending or soldering of the leads.

2. What is the general information specified in ordering an IC?
a) Temperature range
b) Device type
c) Package type
d) All of the mentioned
Answer: d
Explanation: Generally, in ordering an IC, all the three informations must be specified.

3. Find the ordering information for µA741TC.
a) Sprague 741 DIP with Industrial temperature range
b) Intersil 741 DIP with commercial temperature range
c) Fairchilds 741 DIP with commercial temperature range
d) Texas instrument 741 metal can with Industrial temperature range
Answer: c
Explanation: Here "µA" represents the identifying initials used by Fairchild,
T represents Mini DIP package and C represents Commercial temperature range.

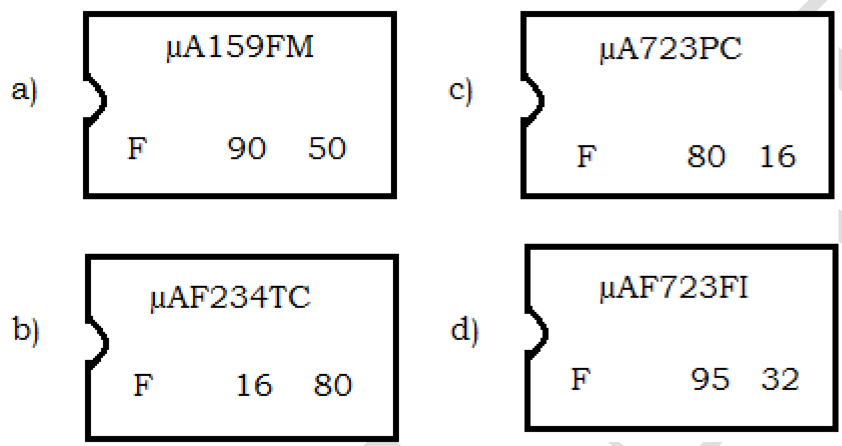
4. How a Motorola IC with plastic DIP and commercial temperature range is ordered?
a) ICLxxxP -> 0^o to 75^oc
b) CAxxE -> -55^o to $+125^o$c
c) LMxxxxA -> -40^o to $+85^o$c
d) MCxxxP -> 0^o to 70^oc
Answer: d
Explantion: The ordering format for a typical Motorola IC is,
MCxxxx –> Device type
P –> Package type(Plastic DIP)
0^o to 70^oc –> Temperature range (Commercial).

5. What does the 1-2-3 numbering system used in National Semiconductor IC denotes
a) Validity in years
b) Temperature range
c) Package type
d) Ordering information
Answer: c

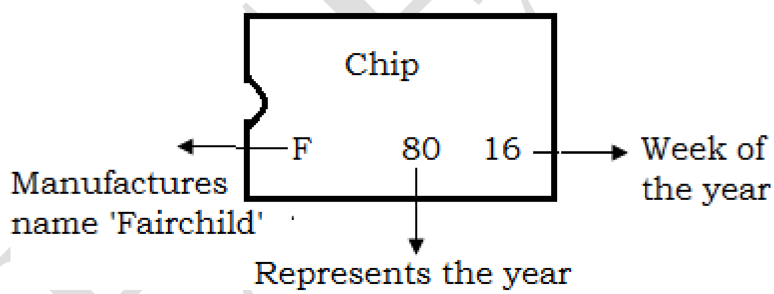
Explanation: In National linear ICs, a 1-2-3 numbering system is used to represent the temperature range.

6. How does a industrial temperature range device in National Semiconductor IC is represented?
a) LM305
b) LM101
c) LM201
d) All of the mentioned
Answer: c
Explanation: In LM201, the number 2 denotes an industrial temperature range device.

7. Use device identification method to find the IC of Fairchild chip manufactured in the year 1980.



Answer: b
Explanation: In the chip, 80 represent the manufactured year



8. Dual-In-Line pack is considered to be suitable for mounting because,
a) Easy to handle
b) Fits mounting hardware
c) Inexpensive
d) All of the mentioned
Answer: c
Explanation: DIP pack is easy to handle, fit standard mounting hardware and is inexpensive when moulded on plastic.

9. What is the use of notch and dot in DIP ICs?
a) Determine the pin configuration
b) Designed to represent device type
c) Represent property of IC
d) Find the pin number
Answer: d
Explanation: A notch and dot as viewed form top view is used to find the pin terminal. The terminals are numbered counter clockwise.

10. How an eight pin Dual-In-Line Package is shortly named
a) 8p DIP
b) Maxi DIP
c) Mini DIP
d) ES DIP
Answer: c
Explanation: An eight pin Dual-In-Line Package is called as Mini DIP as it is used for devices with minimum number of inputs and outputs.

11. Which package type is chosen for military purposes?
a) Ceramic DIP
b) Plat pack
c) Metal can pack
d) Plastic DIP
Answer: a
Explanation: Ceramic DIP can be used for high temperature and high performance equipment.

12. A Dual-In-Line Package is usually referred to as
a) DIP_n
b) $_nDIP$
c) DIP^n
d) All of the mentioned
Answer: a
Explanation: A Dual-In-Line Package is usually referred to as DIP_n. Where, n represent the number of pin terminals in the IC.

13. Which type of DIP IC dissipates more heat?
a) Ceramic DIP
b) Plastic DIP
c) Metal DIP
d) None of the mentioned
Answer: b
Explanation: Plastic DIP are cheaper than metal or ceramic DIP, but are not regarded as satisfactory in extremes of temperature.

14. Choose the type of package used for Airborne application?
a) DIP package

b) Metal can package
c) Flat pack
d) Transistor pack
Answer: c
Explanation: The flat pack is more reliable and lighter than a comparable DIP package and therefore is suited for airborne application.

15. How a choice is made, if all three package types are available?
a) Based on cost
b) Based on fabrication
c) Based on Experimentation usage
d) All of the mentioned
Answer: d
Explanation: When all three packages are available for a specific application, the choice can be made based on the relative cost, ease of fabrication and breadbording the IC.

16. How many temperature grades are available for IC?
a) Two
b) Three
c) Four
d) Five
Answer: b
Explanation: All ICs manufactured fall into one of the three basic temperature grades. They are military, industrial and commercial temperature range.

17. ICs used for industrial application will have temperature range from
a) -55^o to $+85^o$c
b) 90^o to 155^oc
c) 10^o to 100^oc
d) -20^o to $+85^o$c
Answer: d
Explanation: The industrial temperature range is from -20^o to $+85^o$c.

18. Find the types of temperature range used for an IC, which can be used only up to 75^oc?
a) Industrial temperature range
b) Commercial temperature range
c) Military temperature range
d) All of the mentioned
Answer: b
Explanation: Commercial grade IC can be used up to 75^oc. It has the worst tolerance among the three types and is the cheapest available IC.

19. Which grade device is selected for superior quality performance?
a) Military grade IC
b) Industrial grade IC
c) Commercial grade IC

d) None of the mentioned
Answer: a
Explanation: The military grade devices are always of superior quality, with tightly controlled parameters and consequently cost more.

20. In ordering an IC, the device type is represented as
a) Numbers
b) Symbols
c) Alphabets
d) Alphanumeric characters
Answer: d
Explanation: The device type is a group of alphanumeric characters. For example, 741 IC is represented as µA741, LM741 and MC1741.

21. How many gates per chip are used in first generation Integrated Circuits?
a) 3-30
b) 30-300
c) 300-3000
d) More than 3000
Answer: a
Explanation: The first generation ICs belongs to small scale integration, which consists of 3-30 gates per chip (approximately).

22. Find the chip area for a Medium Scale Integration IC?
a) 8 mm^3
b) 4 mm^2
c) 64 mm^3
d) 16 mm^2
Answer: d
Explanation: The approximate length and breadth of Medium Scale Integration would be 4 mm. Therefore, its area is given as = length × breadth = 4mm × 4mm = $16mm^{2.}$

23. The number of transistors used in Very Large Scale Integration is
a) 10^7 transistors/chip
b) $10^6 – 10^7$ transistors/chip
c) $20^3 – 10^5$ transistors/chip
d) $10^2 – 20^3$ transistors/chip
Answer: c
Explanation: Very Large Scale Integration (VLSI) ICs are fabricated using more than 3000 gates/chip, which is equivalent to 20,000 – 1,00,00,00 transistors/chip.

24. What type of integration is chosen to fabricate Integrated Circuits like Counters, multiplexers and Adders?
a) Small Scale Integration (SSI)
b) Medium Scale Integration (MSI)
c) Large Scale Integration (LSI)

d) Very Large Scale Integration (VLSI)
Answer: b
Explanation: Fabrication of ICs like counter, multiplexers and Adders requires 30-300 gates per chip. Therefore, Medium Scale Integration is best suitable.

25. Determine the chip area for Large Scale Integration ICs.
a) 1,00,000 mil^2
b) 10,000 mil^2
c) 1,60,000 mil^2
d) 16,000 mil^2
Answer: c
Explanation: The chip area for a Large Scale Integration IC is 1 cm^2.
=> Area of LSI = 10mm × 10mm = 1cm × 1 cm = $1cm^2$.
=> $1{,}60{,}000mil^2$ (1cm=400mil).

26. Ultra Large Scale Integration are used in fabrication of
a) 8-bit microprocessors, RAM, ROM
b) 16 and 32- bit microprocessors
c) Special processors and Smart sensors
d) All of the mentioned
Answer: c
Explanation: Ultra Large Scale Integration have nearly $10^6 – 10^7$ transistors/chip. Hence, it is possible to fabricate smart sensors and special processor.

27. The concept of Integrated circuits was introduced at the beginning of 1960 by
a) Texas instrument and Fairchild Semiconductor
b) Bell telephone laboratories and Fair child Semiconductor
c) Fairchild Semiconductor
d) Texas instrument and Bell telephone Laboratories
Answer: a
Explanation: The concept of Integrated circuits was introduced by Texas instrument and Fairchild Semiconductor, whereas Bell telephone laboratories developed the concept of transistors.

28. Which process is used to produce small circuits of micron range on silicon wafer?
a) Photo etching
b) Coordinatograph
c) Photolithography
d) Ion implantation
Answer: c
Explanation: It is possible to fabricate as many as 10,000 transistors on a 1cmX1cm chip, using photolithography process.

29. Mention the technique used in photolithography process
a) X-ray lithographic technique
b) Ultraviolet lithographic technique

c) Electron beam lithographic technique
d) All of the mentioned
Answer: d
Explanation: All these techniques are used to produce device dimension as small as 2µm or even down to sub micron range (<1µm).

Differential Amplifier

1. A Differential Amplifier should have collector resistor's value (RC1 & RC2) as
a) 5kΩ, 5kΩ
b) 5Ω, 10kΩ
c) 5Ω, 5kΩ
d) 5kΩ, 10kΩ
Answer: a
Explanation: The values of collector current will be equal in differential amplifier (RC1=RC2).

2. A Differential Amplifier amplifies
a) Input signal with higher voltage
b) Input voltage with smaller voltage
c) Sum of the input voltage
d) None of the Mentioned
Answer: d
Explanation: The purpose of differential amplifier is to amplify the difference between two signals.

3. The value of emitter resistance in Emitter Biased circuit are RE1=25kΩ & RE2=16kΩ. Find RE
a) 9.756kΩ
b) 41kΩ
c) 9.723kΩ
d) 10kΩ
Answer: a
Explanation: In emitter biased circuit, RE1 & RE2 is connected in parallel combination.
⇒ RE = RE1 II RE2 = (RE1× RE2)/(RE1+RE2) = (25kΩ×16kΩ)/(25kΩ+16kΩ) = 9.7561kΩ.

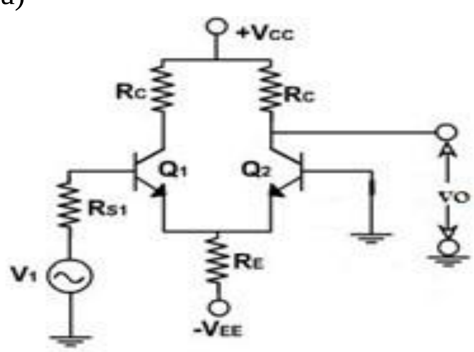
4. If output is measured between two collectors of transistors, then the Differential amplifier with two input signal is said to be configured as
a) Dual Input Balanced Output
b) Dual Input Unbalanced Output
c) Single Input Balanced Output
d) Dual Input Unbalanced Output
Answer: a
Explanation: When two input signals are applied to base of transistor, it is said to be Dual Input. When both collectors are at same DC potential with respect to ground, then it is said to be Balance Output.

5. A differential amplifier is capable of amplifying
a) DC input signal only
b) AC input signal only
c) AC & DC input signal
d) None of the Mentioned
Answer: c
Explanation: Direct connection between stages removes the lower cut off frequency imposed by coupling capacitor; therefore it can amplify both AC and DC signal.

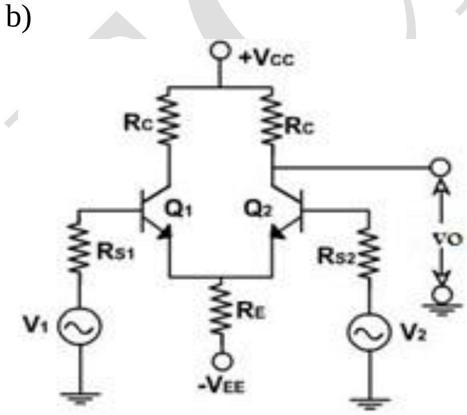
6. In ideal Differential Amplifier, if same signal is given to both inputs, then output will be
a) Same as input
b) Double the input
c) Not equal to zero
d) Zero
Answer: d
Explanation: In ideal amplifier, Output voltage
⇒ Vout = Vin1-Vin2.

7. Find the Single Input Unbalance Output configuration in following circuit diagrams :

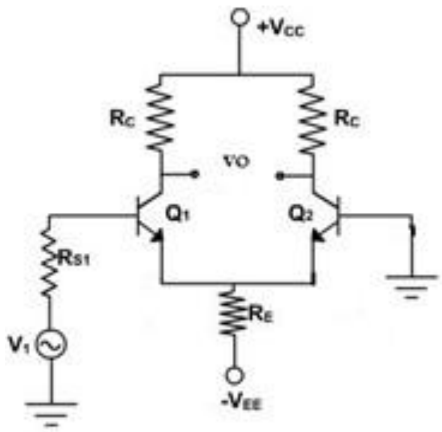
a)



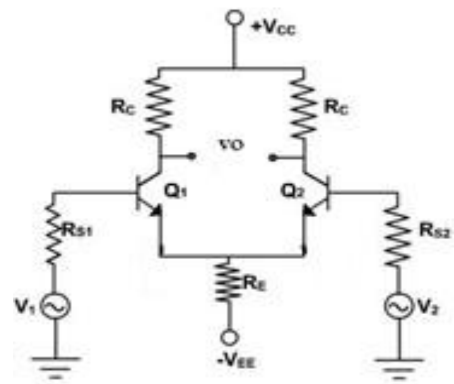
b)



c)



d)



Answer: c
Explanation: Circuit c has only single input (V1) and output is measure only at one of the collector with respect to ground.

8. An emitter bias Dual Input Balanced Output differential amplifier has VCC=20v, β=100, VBE=0.7v, RE=1.3kΩ. Find IE
a) 7.42mA
b) 9.8mA
c) 10mA
d) 8.6mA
Answer: a
Explanation: Emitter current can be found out by substituting the values in the equation,
⇒ IE = (VEE-VBE)/(2RE) = (20v-07v)/(2×1.3kΩ) = 7.42mA.

9. Find IC, given VCE=0.77v, VCC=10v, VBE=0.37v and RC=2.4kΩ in Dual Input Balanced Output differential amplifier
a) 0.4mA

b) 0.4A
c) 4mA
d) 4A
Answer: c
Explanation: Substitute the values in collector to emitter voltage equation,
VCE= VCC+ VBE-RC IC
⇒IC = (VCC-VCE+VBE)/RC = (10v-0.77v+0.37v)/2.4kΩ = 4mA

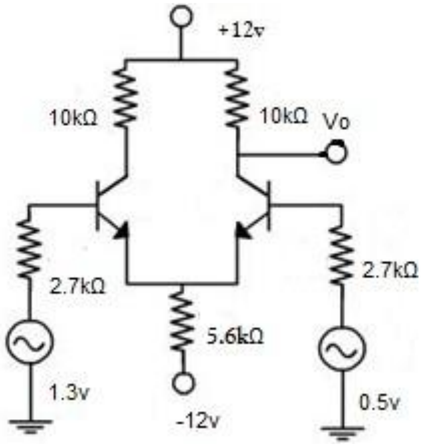
10. Find the correct match

Configuration	**Voltage gain and Input resistance**
1. Single Input Unbalanced Output	i. $A_d = Rc/re$, $R_{i1}\ R_{i2} = 2\beta_{ac}RE$
2. Dual Input Balanced Output	ii. $A_{d} = Rc/2re$, $Ri1\ Ri2 = 2\beta acRE$
3. Single Input Balanced Output	iii. $A_d = Rc/re$, $R_i = 2\beta_{ac}RE$
4. Dual Input Unbalanced Output	iv. $A_d = Rc/2re$, $R_i = 2\beta_{ac}RE$

a) 1-i , 2-iii, 3-iv, 4-ii
b) 1-iv, 2-ii, 3-iii, 4-i
c) 1-ii, 2-iv, 3-i , 4-iii
d) 1-iii, 2-i, 3-ii, 4-iv
Answer: d
Explanation: Properties of differential amplifier circuit configuration.

11. Obtain the collector voltage, for collector resistor (RC) =5.6kΩ, IE=1.664mA and VCC=10v for single input unbalanced output differential amplifier
a) 0.987v
b) 0.682v
c) 0.555v
d) None of the mentioned
Answer: b
Explanation: Substitute the given values in collector voltage equation,
VC= VCC – RC×IC
⇒ VC= 10v – 5.6kΩ×1.664mA (∵ IC ≅ IE)
⇒ VC= 0.682v.

12. For the circuit shown below, determine the Output voltage (Assume β=5, differential input resistance=12 kΩ)



a) 4.33v
b) 2.33v
c) 3.33v
d) 1.33v

Answer: c
Explanation: From the circuit dig, RC=10kΩ, Vin1= 1.3v and Vin2=0.5v,
Differential input resistance = 2 βre,
⇒ 12kΩ = 2×5×Re
⇒ Re = 1.2 kΩ
Output voltage Vo = RC/2Re(Vin1-Vin2)
⇒ Vo = 10kΩ/(2 ×1.2kΩ) × (1.3v-0.5v)
⇒ Vo = 3.33v.

13. In a Single Input Balanced Output Differential amplifier, given VCC=15v, RE = 3.9kΩ, VCE=2.4 v and re=250Ω. Determine Voltage gain
a) 26
b) 56
c) 38
d) 61Answer: a
Explanation: In single Input Balance Output amplifier,
⇒ IE = (VEE-VBE)/2RE
=(15v-0.7v)/(2×3.9kom)= 1.83mA (∵VCC=VEE)
From the equation, VCE = VCC +VBE-RC×IC
⇒ RC = (14.3v – 2.4v)/1.83mA = 6.5kΩ
The voltage gain, Vo
⇒ Vo = RC/re
= 6.5kΩ/250Ω = 26(no units).

Operational Amplifier

1. Which is not the internal circuit of operational amplifier?
a) Differential amplifier
b) Level translator
c) Output driver
d) Clamper
Answer: d
Explanation: Clamper is an external circuit connected at the output of Operational amplifier, which clamp the output to desire DC level.

2. The purpose of level shifter in Op-amp internal circuit is to
a) Adjust DC voltage
b) Increase impedance
c) Provide high gain
d) Decrease input resistance
Answer: a
Explanation: The gain stages in Op-amp are direct coupled. So, level shifter is used for adjustment of DC level.

3. How a symmetrical swing is obtained at the output of Op-amp
a) Providing amplifier with negative supply voltage
b) Providing amplifier with positive voltage
c) Providing amplifier with positive& negative voltage
d) None of the mentioned
Answer: c
Explanation: For example, consider a single voltage supply +15v. During positive half cycle the output will be +5v and -10v during negative half cycle.
Therefore, the maximum peak to peak output swing, -5v (-10v) = -15v (Asymmetrical swing).
So, to get symmetrical swing both positive and negative supply voltage with bias point fixed suitably is required.

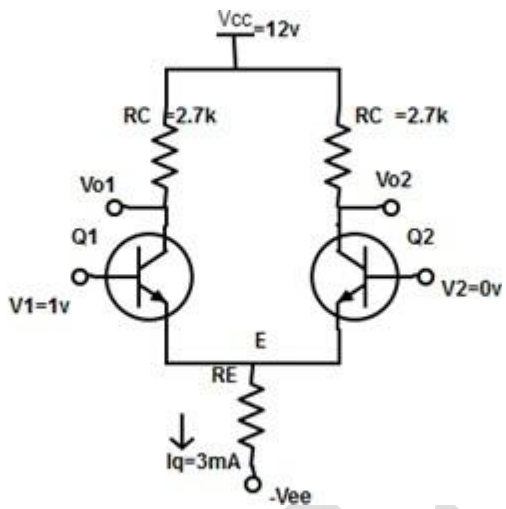
4. What is the purpose of differential amplifier stage in internal circuit of Op-amp?
a) Low gain to differential mode signal
b) Cancel difference mode signal
c) Low gain to common mode signal
d) Cancel common mode signal
Answer: d
Explanation: Any undesired noise, common to both of the input terminal is suppressed by differential amplifier.

5. Which of the following is not preferred for input stage of Op-amp?
a) Dual Input Balanced Output
b) Differential Input Single ended Output
c) Cascaded DC amplifier

d) Single Input Differential Output

6. What will be the emitter current in a differential amplifier, where both the transistor are biased and matched? (Assume current to be I_Q)
a) $I_E = I_Q/2$
b) $I_E = I_Q$
c) $I_E = (I_Q)^2/2$
d) $I_E = (I_Q)^2$
Answer: a
Explanation: Due to symmetry of differential amplifier circuit, current I_Q divides equally through both transistors.

7. From the circuit, determine the output voltage (Assume α_F=1)



a) V_{O1}=3.9v , V_{O2}=12v
b) V_{O1}=12v , V_{O2}=3.9v
c) V_{O1}=12v , V_{O2}=0v
d) V_{O1}=3.9v , V_{O2}=-3.9v
Answer: b
Explanation: The voltage at the common emitter 'E' will be -0.7v, which make Q_1 off and the entire current will flow through Q_2.
$\Rightarrow V_{O1} = VCC\ V_{O2} = VCC-\alpha_F \times I_Q \times RC$,
$\Rightarrow V_{O1} = 12v$, $V_{O2} = 12v-1\times3mA\times2.7k = 3.9v$.

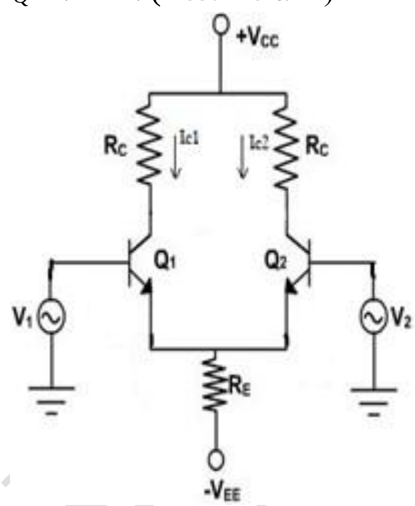
8. At what condition differential amplifier function as a switch
a) $4V_T < V_d < -4V_T$
b) $-2V_T \leq V_d \leq 2V_T$
c) $0 \leq V_d < -4V_T$
d) $0 \leq V_d \leq 2V_T$
Answer: a
Explanation: For $V_d > 4V_T$, the output voltage are V_{O1} = VCC, V_{O2}= VCC-$\alpha_F I_Q$RC. Therefore, a

transistor Q_1 will be ON and Q_2 will be OFF. Similarly for $V_d > -4V_T$, both transistors Q_2 & Q_1 will be ON.

9. For $V_d > \pm 4V_T$, the function of differential amplifier will be
a) Switch
b) Limiter
c) Automatic gain control
d) Linear Amplifier
Answer: b
Explanation: At this condition, input voltage of the amplifier is greater than ±100mv and thus acts as a limiter.

10. Change in value of common mode input signal in differential pair amplifier make
a) Change in voltage across collector
b) Slight change in collector voltage
c) Collector voltage decreases to zero
d) None of the mentioned
Answer: a
Explanation: In differential amplifier due to symmetry, both transistors are biased and matched. Therefore, Voltage at each collector will be same.

11. Find collector current I_{C2}, given input voltages are V_1=2.078v & V_2=2.06v and total current I_Q=2.4mA. (Assume α=1)



a) 0.8mA
b) 1.6mA
c) 0.08mA
d) 0.16mA
Answer: a
Explanation: Collector current, $I_{C2}=\alpha_F \times I_Q/(1+e^{V_d/V_T})$,
V_T = Volts equivalent of temperature = 25mv,
⇒ $V_d = V_1 - V_2$ =2.078v-2.06v=0.018v (equ1)
Substituting equation 1,
⇒ V_d/V_T = 0.018v/25mv = 0.72v (equ2)

Substituting equation 2,
$\Rightarrow I_{C2}= 1\times 2.4mA/(1+e^{0.72}) = 2.4mA/(1+2.05) = 0.8mA$.

12. A differential amplifier has a transistor with $\beta_0= 100$, is biased at $I_{CQ} = 0.48mA$. Determine the value of CMRR and A_{CM}, if RE =7.89kΩ and RC = 5kΩ.
a) 49.54 db
b) 49.65 d
c) 49.77 db
d) 49.60 db
Answer: b
Explanation: Differential mode gain, $A_{DM}= -g_mRC$ and Common mode gain,
$\Rightarrow A_{CM}= -(g_mRC)/(1+2g_mRE)$
(for $\beta_0 \gg 1$).
Substituting the values,
$\Rightarrow g_m= I_{CQ}/V_T = 0.48mA/25mv=19.2\times 10^{-3}\Omega^{-1}$
$\Rightarrow A_{DM}= -g_m\times RC= -19.2\times 10^{-3}\Omega^{-1}\times 5k\Omega= -96$
$\Rightarrow A_{CM}= -(g_mRC)/(1+2g_mRE)= -(19.2\times 10^{-3}\Omega^{-1}\times 5k\Omega) /(1+2\times -\Rightarrow 19.2\times 10^{-3}\Omega^{-1}\times 7.89k\Omega) = -0.3158$
CMRR = -96/-0.3158= 303.976
$=20\log_{10}303.976$
=49.65db

13. How are the arbitrary signal represented, that are applied to the input of transistor? (Assume common mode signal and differential mode signal to be V_{CM} & V_{DM} respectively).
a) Sum of V_{CM} & V_{DM}
b) Difference of V_{CM} & V_{DM}
c) Sum and Difference of V_{CM} & V_{DM}
d) None of the mentioned
Answer: c
Explanation: In practical situation, arbitrary signal are signal are represented as Sum and Difference of common mode signal and differential mode signal.

14. How the differential mode gain is expressed using 'h' parameter for a single ended output?
a) $– h_{fe}RC/h_{ie}$
b) $1/2\times(h_{fe}RC)/h_{ie}$
c) $– 1/2\times h_{fe}RC$
d) None of the mentioned
Answer: b
Explanation: Formula for differential mode gain using 'h' parameter model for a single ended output.

15. Find Common Mode Rejection Ration, given g_m =16MΩ^{-1}, RE=25kΩ
a) 58 db
b) 40 db
c) 63 db

d) 89 db
Answer: a
Explanation: Formula for Common Mode Rejection Ration, CMRR= $1+2g_mRE$,
⇒ CMRR = $1+(2\times16M\Omega^{-1}\times25k\Omega)$
= 801 = 20log 801 = 58.07 db.

16. In differential amplifier the input are given as $V_1=30\sin\Pi(50t)+10\sin\Pi(25t)$, $V_2=30\sin\Pi(50t)-10\sin\Pi(25t)$, $\beta_0=200$,RE =1kΩ and RC = 15kΩ. Find the output voltages V_{01}, V_{02} & $g_m=4M\Omega^{-1}$
a) $V_{01}=-60[10\sin\Pi(25t)]-6.637[30\sin\Pi(50t)]$, $V_{02}=60[10\sin\Pi(25t)]-6.637[30\sin\Pi(50t)]$.
b) $V_{01}=-6.637[10\sin\Pi(25t)]-60[30\sin\Pi(50t)]$, $V_{02}=6.637[10\sin\Pi(25t)]-60[30\sin\Pi(50t)]$.
c) $V_{01}=-60[30\sin\Pi(50t)]-6.637[10\sin\Pi(25t)]$, $V_{02}=60[30\sin\Pi(50t)]-6.637[10\sin\Pi(25t)]$.
d) $V_{01}=-6.637[30\sin\Pi(50t)]-60[10\sin\Pi(25t)]$, $V_{02}=6.637[30\sin\Pi(50t)]-60[10\sin\Pi(25t)]$.
Answer: a
Explanation: Differential mode gain, $A_{DM}=-g_m RC$,
⇒ $A_{DM}=-4M\Omega^{-1}\times15k\Omega=60$
⇒ $r_\Pi=\beta_0/g_m=200/4M\Omega^{-1}=50k\Omega$
Common mode gain, $A_{CM}=-\beta_o\times RC/r_\Pi+(\beta_O+1)\times RE$
⇒ $A_{CM}=-200\times15k\Omega/50k\Omega+2(1+200)\times1k\Omega=-6.637$
Common mode signal, $V_{CM}=(V_1+V_2)/2=30\sin\Pi(50t)$
Differential mode signal, $V_{DM}=(V_1-V_2)/2=10\sin\Pi(25t)$
Output voltages are given as
⇒ $V_{01}=A_{DM})\times V_{DM})+A_{CM}\times V_{CM}$
= $-60[10\sin\Pi(25t)]-6.637[30\sin\Pi(50t)]$,
⇒ $V_{02}=-A_{DM}\times V_{DM}+A_{CM}\times V_{CM}$
= $60[10\sin\Pi(25t)]-6.637[30\sin\Pi(50t)]$.

17. If the value of Common Mode Rejection Ratio and Common Mode Gain are 40db and -0.12 respectively, then determine the value of differential mode gain
a) 0.036
b) -1.2
c) 4.8
d) 12
Answer: d
Explanation: Common mode rejection ratio, CMRR =$\log^{-1}\times(40/20)=100$
⇒ CMRR =$(|A_{DM}|/|A_{CM}|)$
⇒ $|A_{DM}|=100\times0.12=12$.

18. To increase the value of CMRR, which circuit is used to replace the emitter resistance Re in differential amplifier?
a) Constant current bias
b) Resistor in parallel with Re

c) Resistor in series with Re
d) Diode in parallel with Re
Answer: a
Explanation: Constant current bias offers extremely large resistor under AC condition and thus provide high CMRR value.

19. What is the purpose of diode in differential amplifier with constant current circuit?
a) Total current independent on temperature
b) Diode is dependent of temperature
c) Transistor is depend on temperature
d) None of the mentioned
Answer: a
Explanation: The base emitter voltage of transistor (VBE) in constant current circuit by 2.5mv/^{o}c, thus diode also has same temperature. Hence two variations cancel each other and total current I_Q become in depend of temperature.

20. How to improve CMRR value
a) Increase common mode gain
b) Decrease common mode gain
c) Increase Differential mode gain
d) Decrease differential mode gain
Answer: b
Explanation: For a large CMRR value, A_{CM} should be small as possible.

21. Define total current (I_Q) equation in differential amplifier with constant current bias current
a) $I_Q=1/R_3\times(VEE/R_1+R_2)$
b) $I_Q=(VEE\times R_2)/(R_1+R_2)$
c) $I_Q=1/R_3\times(VEE\times R_2/R_1+R_2)$
d) $I_Q)=R_3\times(VEE/R_1+R_2)$
Answer : c
Explanation: The equation for total current is obtained by applying Kirchhoff's Voltage Law to constant current circuit in differential amplifier.

22. Constant current source in differential amplifier is also called as
a) Current Mirror
b) Current Source
c) Current Repeaters
d) All of the mentioned
Answer: a
Explanation: The output current is reflection or mirror of the reference input current. Therefore, the constant current source circuit referred as Current Mirror.

23. When will be the mirror effect valid
a) $\beta\gg1$
b) $\beta=1$
c) $\beta<1$

d) $\beta \neq 1$
Answer: a
Explanation: If value of β is used in the equation, $IC=\beta/(\beta+2)\times I_{ref}$. It almost become unity and the output current become equal to reference current.

24. Calculate the value of reference current and input resistor for current mirror with IC=1.2μA & VCC=12v. Assume β=50.
a) 1.248mA, 9kΩ
b) 1.248mA, 9.6kΩ
c) 1.248mA, 9.2kΩ
d) 1.2mA, 9.6kΩ
Answer: a
Explanation: We know that collector current, $IC=\beta/(\beta+2)\times I_{ref}$,
$\Rightarrow I_{ref}=(\beta+2)/\beta\times IC= (50+2)/50\times 1.2\mu A = 1.248mA$
$\Rightarrow I_{ref}=(VCC-VBE)/R_1$
$\Rightarrow R_1=(12v-07v)/1.248mA = 9.05k\Omega$.

25. Determine the early voltage, if the output resistance is 2.5×2kΩ and input current is 2mA
a) 9.8v
b) 5.6v
c) 7.8v
d) 10v
Answer: d
Explanation: Output resistance, $Ro=V_A/I_{ref}$
$\Rightarrow V_A = Ro\times I_{ref} =2.5\times 2k\Omega\times 2mA =10v$.

26. In practical application of current mirror, early voltage is assumed to be
a) Infinite
b) Zero
c) Unity
d) None of the mentioned
Answer: a
Explanation: Early voltage is assumed to be infinity, so that output resistance tend to infinity and the output current is constant.

27. A widlar current source is used
a) to get low value of current
b) to get high value of CMRR
c) to get low voltage of gain
d) to get high value of Output
Answer: a
Explanation: In the widlar current source Re is added to emitter lead of transistor, which consequently results in smaller output current value.

28. What will be the value of emitter resistance in widlar current source for output current 10mA, having I_{ref}=2.7A

a) 67/(1+1/β)Ω

b) 13/(1+1/β)Ω

c) 14/(1+1/β)Ω

d) 1.36/(1+1/β)Ω

Answer: c

Explanation: Emitter resistor, $RE=V_T/(1+1/\beta)\ I_{ref}\times\ln(I_o/I_{ref})$

$\Rightarrow RE= 0.025/(1+1/\beta)10mA \times \ln(12.7A/10mA) = 14/(1+1/\beta)\Omega$.

29. A current repeater having identical transistor has collector current, I_{C1} =0.39mA. Find I_{C2},I_{C4}& I_{C6}

a) 0.39mA, 0.39mA, 0.78mA

b) 0.78mA, 0.39mA, 0.39mA

c) 0.39mA, 0.78mA, 0.39mA

d) None of the mentioned

Answer: d

Explanation: In current repeater, the current $I_C = I_{C1} = I_{C2} = \cdots = I_{C\,N} \cong I_{ref}$. Where, N – Number of transistors used in current repeater circuit.

30. If the reference and collector current are 0.539mA and 0.49mA respectively, how many transistors are used in current repeater circuit? (Assume β =150)

a) 11

b) 14

c) 10

d) 8

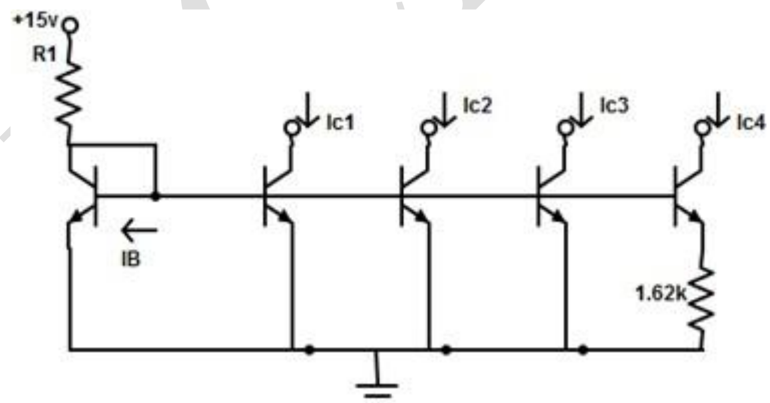
Answer: b

Explanation: The current equation is given as $I_C= I_{ref}\times\beta/(\beta+1+N)$

$\Rightarrow$ 0.49mA= 0.539mA×150/(150+1+N)

$\Rightarrow$ N=14.

31. For the current repeater shown in the circuit, determine I_{C4} value, Where β = 75.



a) 0.035mA

b) 0.028mA

c) 0.04mA

d) 0.052mA
Answer: a
Explanation: The reference current, I_{ref} = VCC-VBE/R_1 =(15v-0.7v)/39kΩ = 0.366mA.
$\Rightarrow I_{ref}=I_C+4\times I_B$
$=I_C(1+1/\beta)$
$\therefore I_C= I_{ref}\times(1+1/\beta)$
$=I_{ref}\times(1+1/\beta)$ = 0.366mA×(1+1/75) =0.347mA
$\Rightarrow I_{C1}=I_{C2}=I_{C3}$=0.347mA
To determine I_{C4},
$RE=V_T/(1+1/\beta)\times I_{C4}\times \ln({}_{C3}/I_{C4})$
⇒ 1.62kΩ = 25mv/(1+1/75)×I_{C4}×ln(0.347mA/I_{C4})
⇒ I_{C4}=0.035mA (find using trial and error method).

32. The requirements for a good current source is the one in which, (Take Output current – I_O and Output resistance – r_O)
a) I_O independent upon current gain and should be low
b) r_O should be very high
c) I_O in the circuit should be low
d) I_O independent upon current gain and r_O should be very high
Answer: d
Explanation: The need for high output resistance current source can be seen because the common mode gain of the differential amplifier can only be reduced by using high resistance current sources.

33. Which current source exhibits a very high output resistance?
a) Simple current mirror
b) Wilson current mirror
c) Widlar current mirror
d) All of the mentioned
Answer: b
Explanation: The output resistance of Wilson current mirror is substantially greater than ≅(β× Output resistance)/2 than Simple or Widlar current source.

34. What will be the overall gain in Darlington circuit, if the individual transistor gain is 200?
a) 10000
b) 40000
c) 8000
d) 1000
Answer: b
Explanation: Overall current gain, $\beta= \beta_1\times\beta_2$ (Multiplication of current gain of individual transistor)
$\Rightarrow \beta=200\times200=40000$

35. To increase the input resistance in differential amplifier, replace the transistor by
a) Current mirror
b) Current repeater

c) Darlington pair
d) All of the mentioned
Answer: c
Explanation: Higher value of input resistance can be obtained by using Darlington pair in place of transistor.

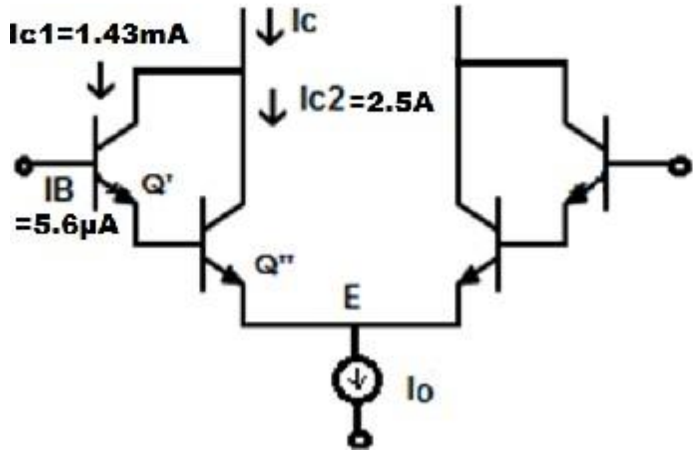
36. What is the drawback in using Darlington pair in differential amplifier?
a) Large current gain
b) Output current in milli ampere
c) Gain is proportional to load resistor
d) High offset voltage
Answer: d
Explanation: Due to cascaded stage, Darlington differential amplifier offers higher offset voltage which is two times larger than ordinary two transistor used in differential amplifier.

37. Determine the amount of shift happens in level shifter?
a) Vcc + 0.7v
b) Vcc – 0.7v
c) -0.7v
d) +0.7v
Answer: c
Explanation: Level shifter is basically a simple type emitter follower. Hence, level shifter also act as a buffer to isolate high gain stages from the output stage. Therefore, the amount of shift obtained is
$V_O – V_i = -V_{BE} = -0.7v$.

38. To increase the input resistance, the differential amplifier replaces transistor by
a) Current mirror
b) Current repeater
c) Darlington pair
d) All of the mentioned
Answer: c
Explanation: Higher value of input resistance can be obtained by using Darlington pair in place of transistor.

39. In Darlington pair differential amplifier the current gain is given as 100. Where I_{B1}=5μA and I_{C1}=0.35mA. Determine I_{C2}
a) 0.5mA
b) 1.5mA
c) 2mA
d) 0.15mA
Answer: d
Explanation: The current gain in Darlington pair differential amplifier is given as $\beta=(I_{C1}+I_{C2})/I_{B1}$.
Substituting the values in the equation, we get
$I_{C2}=(\beta\times I_{B1})-I_{C1}$ =(100×5μA)-0.35mA =0.15mA.

40. In the circuit shown, find the overall current gain?



a) 456218
b) 444878
c) 444210
d) 455734
Answer: b
Explanation: From the circuit given, $I_B = I_{B1} = 5.6\mu A$.
$I_{E1} = I_{B1} + I_{C1} = 1.43mA + 5.6\mu A = 1.435mA$.
$I_{E1} = I_{B2} = 1.435mA$.
The individual current gain values,
$\beta_1 = I_{C1} / I_{B1}$
=> $\beta_1 = 1.43mA/5.6\mu A = 255.36$.
Similarly, $\beta_2 = I_{C2} / I_{B2}$
=> $\beta_2 = 2.5A / 1.435mA = 1742.16$
Therefore, the overall current gain, $\beta = \beta_1 \times \beta_2 = 255.36 \times 1742.16 = 444878$.

41. Introducing FET differential amplifier pair at the input stage of differential amplifier produces
a) High output resistance
b) High input resistance
c) Low input impedance
d) All of the mentioned
Answer: b
Explanation: Input resistance of the order $10^{12}\ \Omega$ is possible with JFET at the input stage of differential amplifier.

42. Why active load is used in amplifier to obtain large gain in intermediate stage of amplifier?
a) To obtain a very large voltage gain
b) To get High input resistance
c) To reduce the noises
d) To increase current gain
Answer: a
Explanation: To increase gain usually large collector resistance value as gain is proportional to

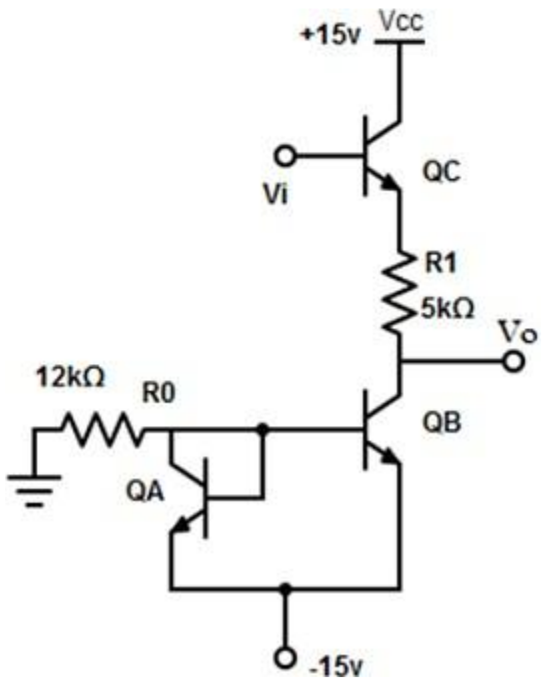
load resistor. However, due to limitation of maximum value load resistor, active loads are used in amplifier to obtain large gain in intermediate stages of amplifier.

43. Which circuit is used as active load for an amplifier
a) Wildar Current source
b) Darlington pair
c) Current Mirror
d) All of the mentioned
Answer: c
Explanation: Current mirror has DC resistance (order of few kΩ), as quiescent voltage across it is a fraction of supply voltage and current in milliampere.

44. What is the equation of load current for a differential amplifier with an active load?
a) $I_L = g_m \times v_d$
b) $I_L = I_q /2$
c) $I_L = \beta \times I_q \times (V_{in1} - V_{in2})$
d) $I_L = 2 \times g_m/(V_{in1} - V_{in2})$
Answer: a
Explanation: The load current is given as product of difference between input & output voltage and transconductance. Therefore, the equation of load current is ,
$I_L = g_m \times v_d$.

45. The input voltage of a difference amplifier are 2.5v and 4.9v. If the transconductance is $0.065\Omega^{-1}$, determine the load current entering the next stage
a) 0.156A
b) 1.56A
c) 0.156mA
d) 15.6μA
Answer: a
Explanation: Load current entering the next stages of amplifier is the sum of individual load current, which is given by $I_L = I_{L1} + I_{L2}$ (Since only two input voltages are given).
$I_L = g_m \times V_{in1} + g_m \times V_{in2}$
$= g_m \times (V_{in1} - V_{in2}) = 0.065\ \Omega^{-1} \times (4.9v-2.5v) = 0.156A$.

46. Calculate the $V_I - V_O$ for the level shifter shown in the figure (Assume identical silicon transistor and very large value of β). Transistor Q_A and Q_B form current mirror.



a) 5.56V
b) 6.00v
c) 7.98v
d) 6.65v
Answer: d
Explanation: Since the transistor Q_A and Q_B form current mirror, $I_{CA}= I_{CB} = I$.
=> $I = (V_{CC} – V_{BE}) / R_0 = (15v-0.7)/12k\ \Omega$ (for β>>1, output current =input current)
=> I= 1.19mA.
The shift in level is given as $V_I – V_O = V_{BE} + I×R_1$ =0.07v+1.19mA×5kΩ =6.65v.

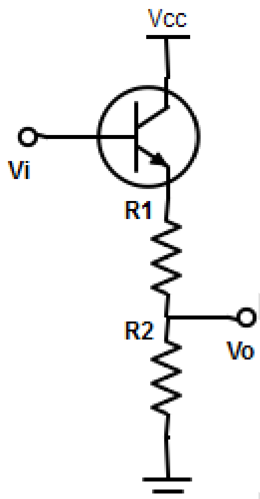
47. Load resistors (Re) is neglected for maximizing the voltage gain in amplifier because,
a) Requires large chip are
b) Requires large power supply
c) Quiescent drop across Re increases
d) All of the mentioned
Answer: d
Explanation: As gain is proportional to load resistor, large resistance value is required. Due to limitation mentioned, it is neglected.

48. What is the need for level shifter in operational amplifier?
a) Level the quiescent voltage
b) Remove distortion at output
c) Limits the output voltage
d) Increase the quiescent voltage
Answer: c
Explanation: Because of direct couple, Dc level rises stages to stage and tends to shift operating point. This limits output swing (Voltage).

49. Limitation of an output stage amplifier, if it emitter follower with complementary transistor
a) Cross-over distortion
b) Low impedance output
c) Shift in level
d) Active load current
Answer: a
Explanation:The limitation in the amplifier is that , the output voltage remains zero until the input voltage exceeds cut in voltage V_{BE}= 0.5v, which is known as cross-over distortion.

50. An output stage amplifier can produce output signal, when the input signal is
a) 0.48v
b) 0.9v
c) 1.2v
d) 0.5v
Answer: c
Explanation: In an Output stage amplifier, due to cross-over distortion output voltage produces input voltage is greater than two times of cut-in voltage which is equal to 1v.
Since, V_{BE}= 0.5v
=> $2\times V_{BE}$= 1v.

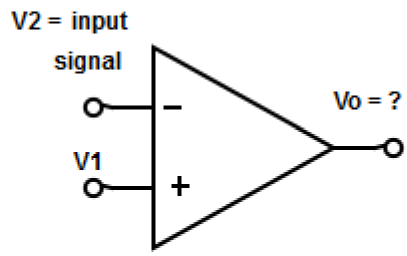
51. Find the disadvantage in the following circuit diagram:



a) Voltage get attenuated by R_1
b) Voltage get attenuated by R_2
c) Voltage get attenuated by R_1 and R_2
d) Voltage shift get increased by the drop across R_1 and R_2
Answer: b
Explanation: The output taken at the junction of R_1 and R_2 increases the voltage shift. However, the disadvantage is that, the signal voltage gets attenuated by R_2.
=> $R_2/(R_1 + R_2)$.

Ideal Operational Amplifier

1. Determine the output from the following circuit



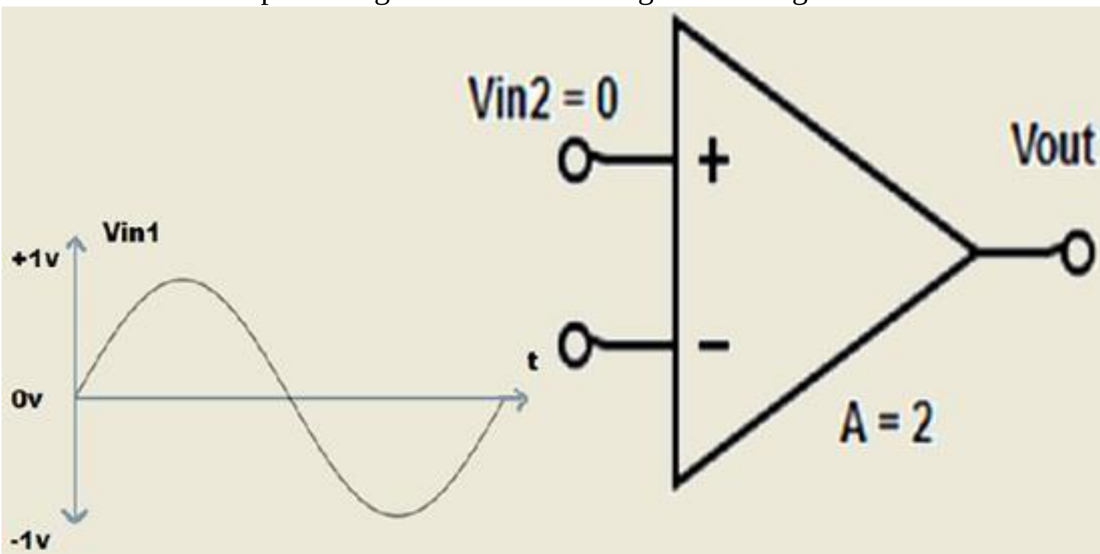
a) 180^{o} in phase with input signal
b) 180^{o} out of phase with input signal
c) Same as that of input signal
d) Output signal cannot be determined
Answer: b
Explanation: The input signal is given to the inverting input terminal. Therefore, the output V_o is 180^{o} out of phase with input signal V_2.

2. Which of the following electrical characteristics is not exhibited by an ideal op-amp?
a) Infinite voltage gain
b) Infinite bandwidth
c) Infinite output resistance
d) Infinite slew rate
Answer: c
Explanation: An ideal op-amp exhibits zero output resistance so that output can drive an infinite number of other devices.

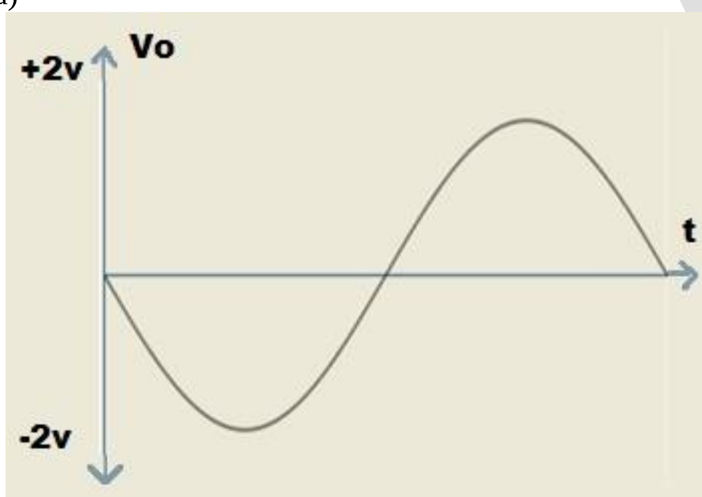
3. An ideal op-amp requires infinite bandwidth because
a) Signals can be amplified without attenuation
b) Output common-mode noise voltage is zero
c) Output voltage occurs simultaneously with input voltage changes
d) Output can drive infinite number of device
Answer: a
Explanation: An ideal op-amp has infinite bandwidth. Therefore, any frequency signal from 0 to ∞ Hz can be amplified without attenuation.

4. Ideal op-amp has infinite voltage gain because
a) To control the output voltage
b) To obtain finite output voltage
c) To receive zero noise output voltage
d) None of the mentioned
Answer: b
Explanation: As the voltage gain is infinite, the voltage between the inverting and non-inverting terminal (i.e. differential input voltage) is essentially zero for finite output voltage.

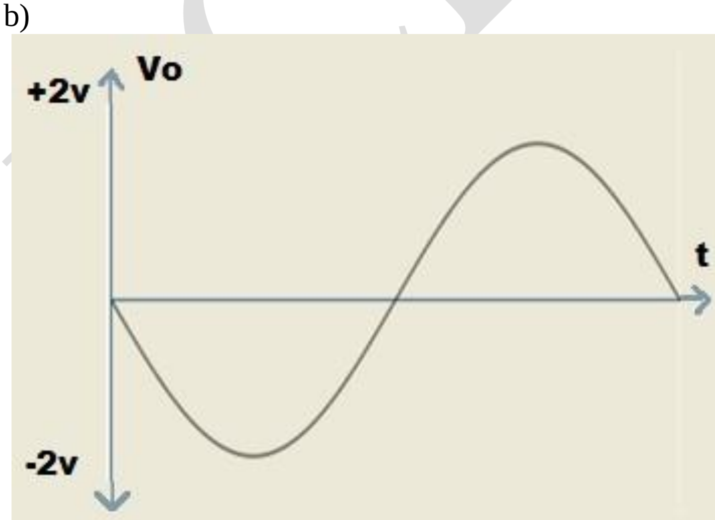
5. Determine the output voltage from the following circuit diagram?



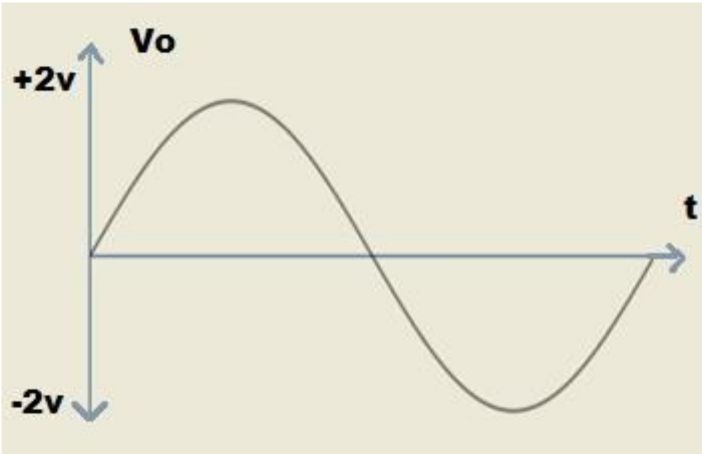
a)



b)



c)



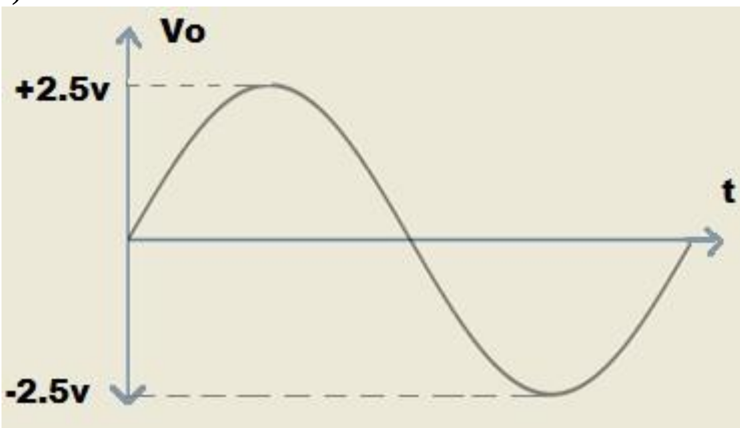
d) None of the mentioned
Answer: c
Explanation: In an ideal op-amp when the inverting terminal is zero. The output will be in-phase with the input signal.

6. Find the output voltage of an ideal op-amp. If V_1 and V_2 are the two input voltages
a) $V_O = V_1 - V_2$
b) $V_O = A\times(V_1 - V_2)$
c) $V_O = A\times(V_1 + V_2)$
d) $V_O = V_1 \times V_2$
Answer: b
Explanation: The output voltage of an ideal op-amp is the product of gain and algebraic difference between the two input voltages.

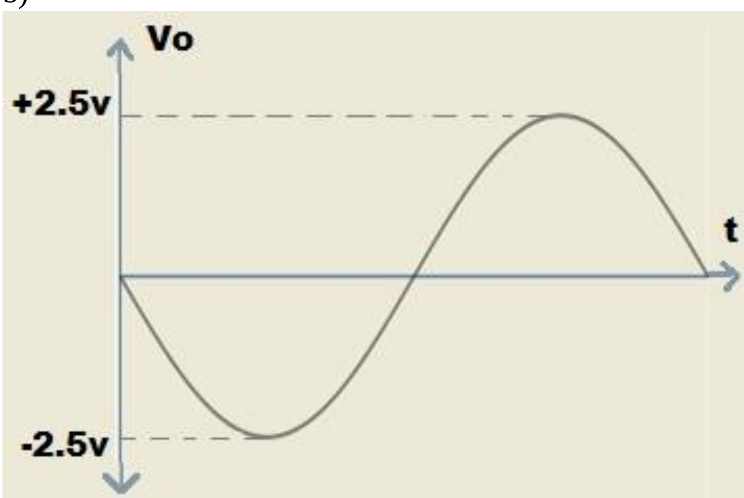
7. How will be the output voltage obtained for an ideal op-amp?
a) Amplifies the difference between the two input voltages
b) Amplifies individual voltages input voltages
c) Amplifies products of two input voltage
d) None of the mentioned
Answer: a
Explanation: Op-amp amplifies the difference between two input voltages and the polarity of the output voltage depends on the polarity of the difference voltage.

8. The signal to an inverting terminal of an ideal op-amp is zero. Find the output voltage, if the other input voltage is

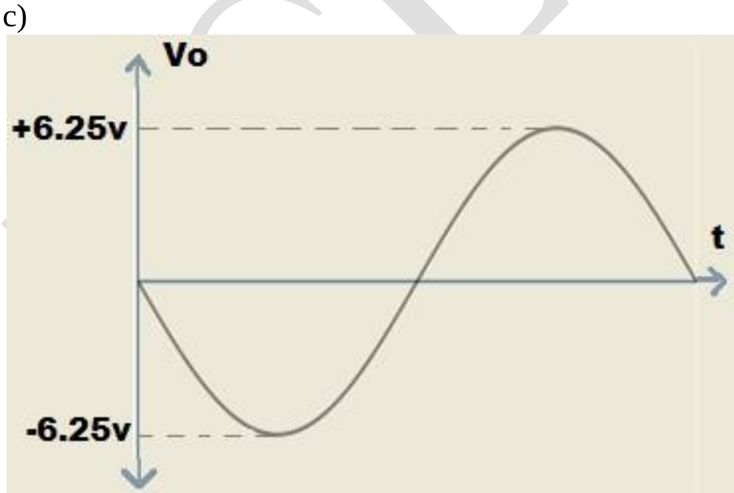
a)



b)



c)



d) Data provided is insufficient

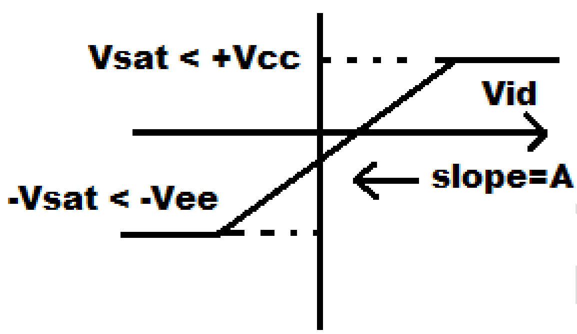
Answer: a

Explanation: Although the output is 180° out of phase with input signal, the gain of the amplifier is not given.

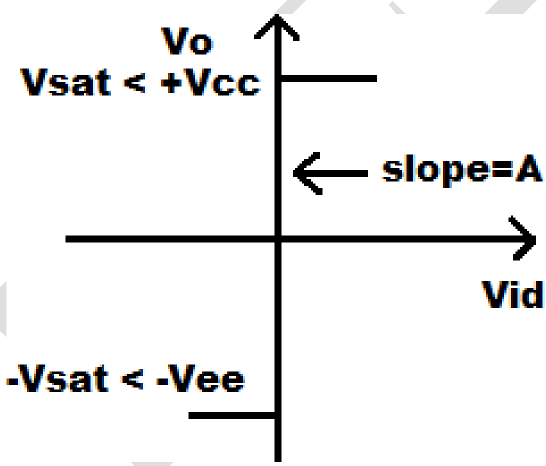
9. Which is not the ideal characteristic of an op-amp?
a) Input Resistance –> 0
b) Output impedance –> 0
c) Bandwidth –> ∞
d) Open loop voltage gain –> ∞
Answer: a
Explanation: Input resistance is infinite so almost any signal source can drive it and there is no loading of the preceding stage.

10. Find the ideal voltage transfer curve of a normal op-amp.

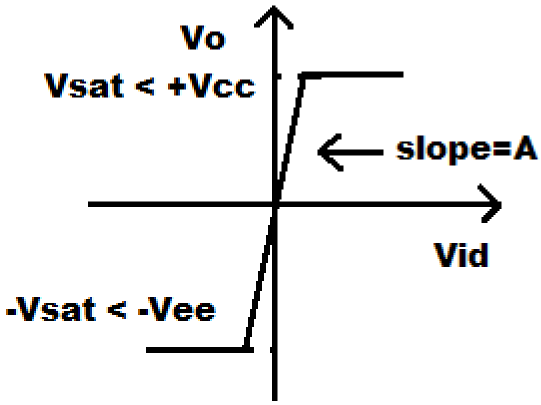
a)



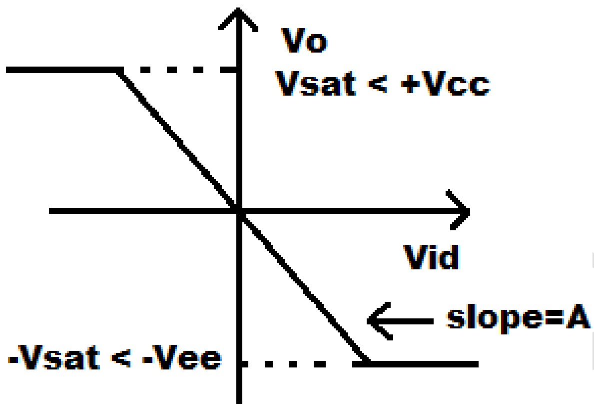
b)



c)



d)



Answer: c
Explanation: The ideal voltage transfer curve would be almost vertical because of the very large value of gain.

11. Find the input voltage of an ideal op-amp. It's one of the inputs and output voltages are 2v and 12v. (Gain=3)
a) 8v
b) 4v
c) -4v
d) -2v
Answer: d
Explanation: The output voltage, $V_O = (Vin_1 – Vin_2)$
=> $12v=3\times(2- Vin_2)$
=> $Vin_2= -2v$.

12. Which factor determine the output voltage of an op-amp?
a) Positive saturation
b) Negative saturation
c) Both positive and negative saturation voltage
d) Supply voltage
Answer: c
Explanation: Output voltage is proportional to input voltage only until it reaches the saturation

voltage. The output cannot exceed the positive and negative saturation voltage. These saturation voltages are specified by an output voltage swing rating of the op-amp for given values of supply voltage

Open loop op-amp configuration

1. Open loop op-amp configuration has
a) Direct network between output and input terminals
b) No connection between output and feedback network
c) No connection between input and feedback network
d) All of the mentioned
Answer: a
Explanation: In an open loop configuration, the output signal is not fed back in any form as part of the input signal and the loop that would have been formed with feedback is open.

2. In which configuration does the op-amp function as a high gain amplifier?
a) Differential amplifier
b) Inverting amplifier
c) Non-inverting amplifier
d) All of the mentioned
Answer: d
Explanation: An op-amp functions as a high gain amplifier when connected in open loop configuration. These three are the open loop configuration of an op-amp.

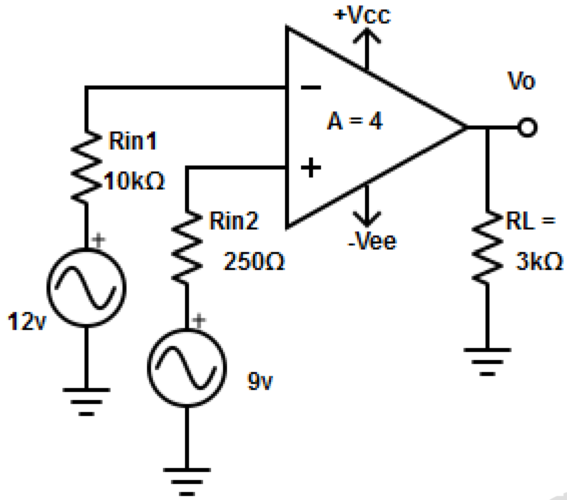
3. How does the open loop op-amp configuration classified?
a) Based on the output obtained
b) Based on the input applied
c) Based on the amplification
d) Based on the feedback network
Answer: b
Explanation: Open loop configurations are classified according to the number of inputs used and the terminal to which the input is applied when a single input is used.

4. What will be the voltage drop across the source resistance of differential amplifier when connected in open loop configuration?
a) Zero
b) Infinity
c) One
d) Greater than one
Answer: a
Explanation: The source resistances are normally negligible compared to the input resistance. Therefore, the voltage drop across input resistors can be assumed to be zero.

5. The output voltage of an open-loop differential amplifier is equal to
a) Double the difference between the two input voltages
b) Product of voltage gain and individual input voltages

c) Product of voltage gain and the difference between the two input voltages
d) Double the voltage gain and the difference between two input voltages
Answer: c
Explanation: The output voltage is equal to the voltage gain times the difference between the two input voltages.

6. Calculate the output voltage for the given circuit.



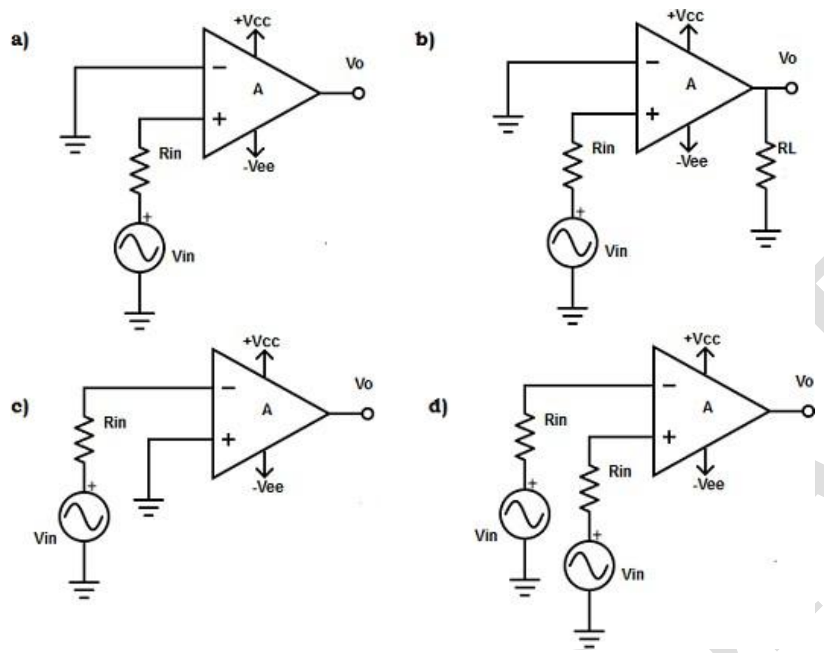
a) $V_o = 7v$
b) $V_o = 5.9v$
c) $V_o = 12v$
d) $V_o = 11.4v$
Answer: c
Explanation: The output voltage, $V_o = A*(V_{in1}-V_{in2})$.(Since, R_{in1} and R_{in2} are negligible compared to input resistance in open loop differential amplifier).
=> $V_o = 4*(12v-9v) = 12v$.

7. Find the output of inverting amplifier?
a) $V_o = AV_{in}$
b) $V_o = -AV_{in}$
c) $V_o = -A(V_{in1} - V_{in2})$
d) None of the mentioned
Answer: b
Explanation: In an inverting amplifier the input signal is amplified by gain A and is also inverted at the output. The negative sign indicates that the output voltage is of opposite polarity.

8. Determine the output voltage for the non-inverting amplifier input voltage 37µVpp sinewave. Assume that the output is a 741.
a) -7.44 Vpp sinewave
b) 74 Vpp sinewave
c) 7.4Vpp sinewave
d) 0.7 Vpp sinewave
Answer: c

Explanation: The output voltage for non-inverting amplifier $V_o = A*V_{in}$ = 200000 * 37µ = 7.4 Vpp sinewave.

9. Find the non-inverting amplifier configuration from the given circuit diagram?



Answer: c

Explanation: In a non-inverting amplifier, the input is applied to the non-inverting input terminal and the inverting terminal is connected to ground.

10. What happen if any positive input signal is applied to open-loop configuration?
a) Output reaches saturation level
b) Output voltage swing's peak to peak
c) Output will be a sine waveform
d) Output will be a non-sinusoidal waveform
Answer: a
Explanation: In open-loop configuration, due to very high gain of the op-amp, any input signal slightly greater than zero drives the output to saturation level.

11. Why open-loop op-amp configurations are not used in linear applications?
a) Output reaches positive saturation
b) Output reaches negative saturation
c) Output switches between positive and negative saturation
d) Output reaches both positive and negative saturation
Answer: c
Explanation: When operated in open loop, the output switches between positive and negative

saturation levels. For this reason, open loop op-amp configurations are not used in linear applications

Feedback Configurations

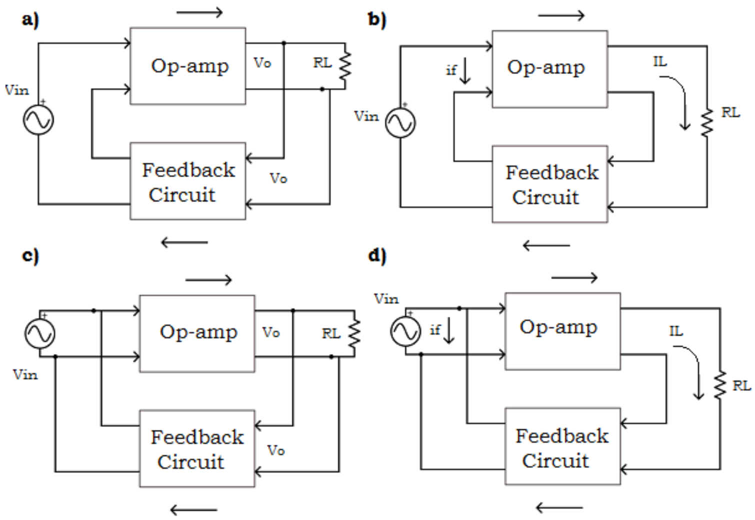
1. A feedback amplifier is also called as
a) Open loop amplifier
b) Closed loop amplifier
c) Feedback network amplifier
d) Looped network amplifier
Answer: b
Explanation: A feedback amplifier is sometimes referred as a closed loop amplifier because the feedback forms a closed loop between input and the output.

2. How many types of configuration are available for feedback amplifier?
a) Six
b) Four
c) Two
d) Eight
Answer: b
Explanation: There are four type of configuration are available. They are voltage series feedback, voltage shunt feedback, Current series feedback and Current shunt feedback.

3. Which of the following is not a feedback configuration?
a) Current-series feedback
b) Voltage-shunt feedback
c) Current-Voltage feedback
c) Current-Shunt feedback
Answer: c
Explanation: In a feedback amplifier, either current or voltage can be fed back to the input, but both current and voltage cannot be feedback simultaneously.

4. When load current flows into the feedback circuit, the configuration is said to be
a) Current-shunt feedback
b) Voltage-shunt feedback
c) Voltage-series feedback
d) All of the mentioned
Answer: b
Explanation: In current-series and current-shunt feedback circuit, the load current flows into the feedback circuit.

5. Find the voltage-series feedback amplifier from the given diagram?



Answer: a

Explanation: The mentioned diagram is the voltage-series feedback amplifier because the voltage across load resistor is the input voltage to the feedback circuit.

6. On what criteria does the feedback amplifier are classified?

a) Signal fed back to input

b) Signal applied to input

c) Signal fed back to output

d) None of the mentioned

Answer: d

Explanation: The feedback amplifiers are classified according to whether the voltage or current is fed back to the input in series or in parallel.

7. The closed loop voltage gain is reciprocal of

a) Voltage gain of op-amp

b) Gain of the feedback circuit

c) Open loop voltage gain

d) None of the mentioned

Answer: b

Explanation: Comparing the equation of closed loop voltage gain (A_F) and the gain of the feedback circuit (B). A_F is reciprocal of B

=> $A_F = 1+(R_F/ R_1)$; $B= R_1/(R_1+ R_F)$

=> $B = 1+(R_1/ R_F)$

Therefore, $A_F = 1/B$.

8. Select the specifications that implies the inverting amplifier?

a) $V_1 = -3v$, $V_2 = -4v$

b) $V_1 = -2v$, $V_2 = 3v$

c) $V_1 = 5v$, $V_2 = 15v$

d) $V_1 = 0v$, $V_2 = 5v$

Answer: d
Explanation: In inverting amplifier, the input is applied to the inverting terminal and the non-inverting terminal is grounded. So,the input applied to inverting amplifier can be $V_1 = 0v$, $V_2 = 5v$

Voltage Series Feedback Amplifier

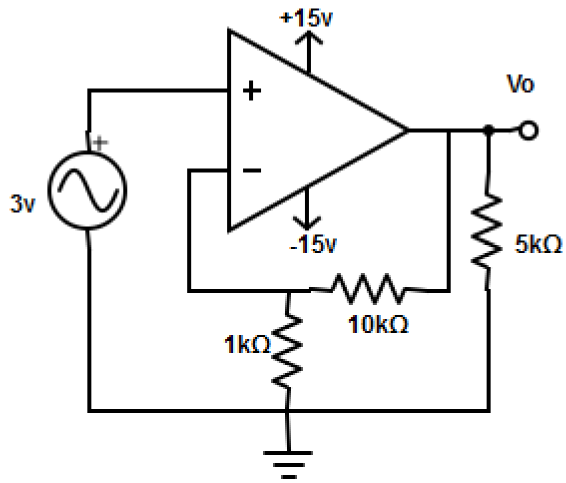
1. Specify the voltage gain of non-inverting amplifier with feedback amplifier with and without feedback?
a) $A= V_o/V_{id}$, $A_F = V_f/V_o$
b) $A= V_f/V_{id}$, $A_F= V_o/V_f$
c) $A= V_o/V_{id}$, $A_F= V_o in$
d) $A= V_f/V_{id}$, $A_F = V_f/V_{in}$
Answer: c
Explanation: The voltage gain of op-amp with feedback is the open loop voltage gain, $A=V_o/V_{id}$. The voltage gain of op-amp without feedback is the closed loop voltage gain, $A_F = V_o/V_{in}$.

2. If the feedback voltage and the output voltage are given as 10v and 4v. Find the gain of the feedback circuit in voltage-series feedback amplifier?
a) 2.5v
b) 40v
c) 3v
d) 6.2v
Answer: a
Explanation: Gain of feedback, $B = V_f/V_o = 10v/4v = 2.5v$.

3. How is the difference voltage calculated in closed loop non-inverting amplifier?
a) $V_{id}= V_o – V_f$
b) $V_{id}= V_{in} – V_f$
c) $V_{id}= V_o – V_{in}$
d) $V_{id}= V_f – V_{in}$
Answer: b
Explanation: Although, the input is given to the non-inverting terminal of op-amp, the difference voltage is equal to the input voltage minus feedback voltage is $V_{id}= V_{in} – V_f$.

4. Why the feedback circuit is said to be negative for voltage series feedback amplifier?
a) Feedback voltage is 180^o out of phase with respect to input voltage
b) Input voltage is 180^o out of phase with respect to feedback voltage
c) Feedback voltage is in same phase with respect to input voltage
d) Input voltage is in same phase with respect to feedback voltage
Answer: a
Explanation: Voltage series feedback amplifier have the difference voltage, $V_{id} = V_{in}-V_f$. Therefore, the feedback voltage always opposes the input voltage and is out of phase by 180^o with respect to input voltage. Hence, the feedback is said to be negative.

5. Determine the closed loop voltage gain from the given circuit. (Where gain of op-amp= 10^5).



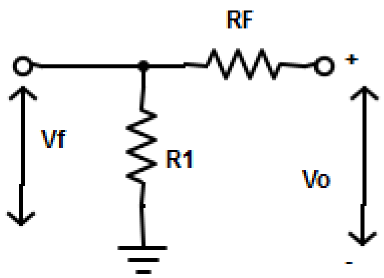
a) 1090.9
b) 9821.43
c) 9166.66
d) 10000
Answer: b
Explanation: The closed loop voltage gain , $A_F = \{[A*(R_4+R_5)]/[(R_F+R_1+(A*R_1)]\}$ = $[10^5*(10k\Omega+1k\Omega)]/[1k\Omega+10k\Omega+(10^5*1k\Omega)] = 11\times10^8/112000$
=> $A_F = 9821.43$.

6. Express closed loop voltage gain (A_F) in terms of open loop gain (A) and feedback circuit gain (B)?
a) $A_F = A/AB$
b) $A_F = 1+(A/AB)$
c) $A_F = A/(1+AB)$
d) $A_F = AB/(1+A)$
Answer: c
Explanation: The closed loop voltage gain in terms of open loop gain and feedback circuit gain is expressed as $A_F = A/(1+AB)$.

7. Which factor determines the gain of the voltage series feedback amplifier?
a) Open loop voltage gain
b) Feedback voltage
c) Ratio of two resistors
d) Gain of feedback circuit
Answer: c
Explanation: In setting the gain of the voltage series feedback amplifier, the ratio of two resistors is important and not the absolute value of these resistors. For example: If a gain of 11 is desired, we choose R_1=1kΩ and R_1=10kΩ or R_1=100Ω and R_F= 1kΩ.

8. For the feedback circuit of voltage series feedback amplifier, find the feedback voltage for the specifications: R_1=1kΩ, R_F = 10kΩ and V_o= 25v.

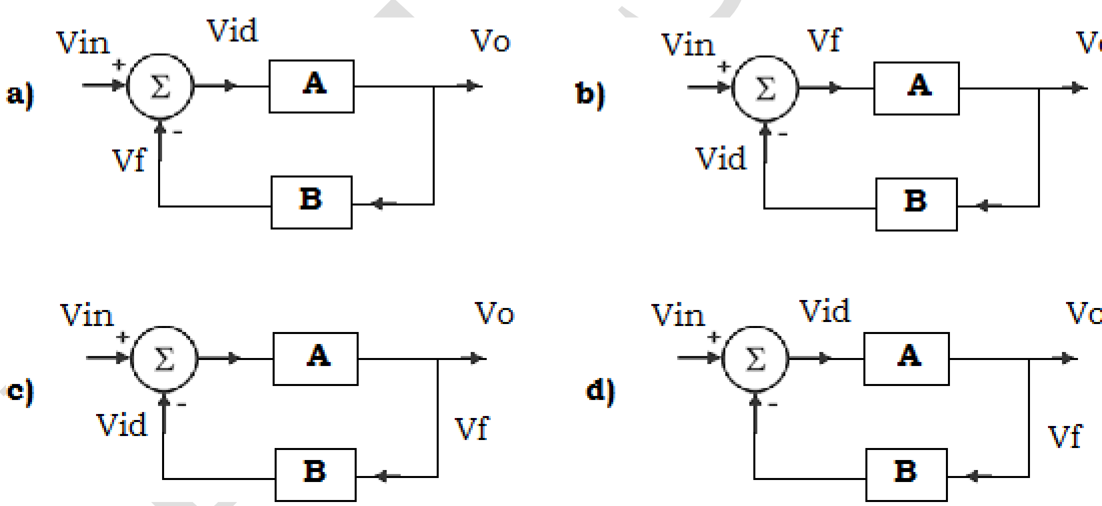
a) 12.5v
b) 22v
c) 0.9v
d) 2.3v
Answer: d



Explanation:
The feedback voltage, $V_f = (R_1*V_o)/(R_1+R_F) = (1k\Omega*25v)/(1k\Omega+10k\Omega) = 2.272v \cong 2.3v$.

9. What must be the value of external components used in voltage series feedback amplifier?
a) Less than 1MΩ
b) Less than 10MΩ
c) Less than 100MΩ
d) Less than 0.1MΩ
Answer: a
Explanation: All external components value should be less than 1MΩ. So, that they do not adversely affect the internal circuitry of the op-amp.

10. Find the block diagram representation of non-inverting amplifier with feedback?



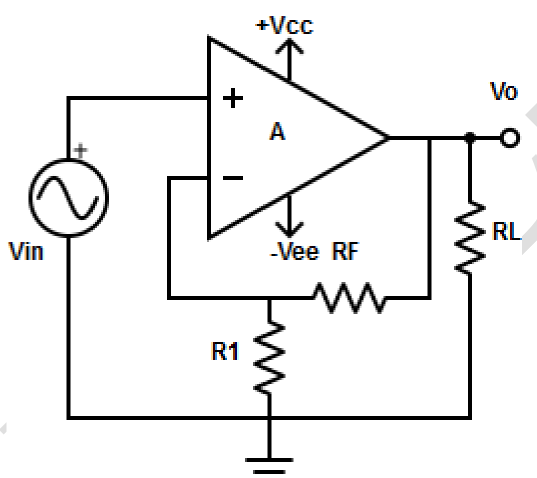
Answer: a
Explanation: The mentioned block diagram is the standard form for representing a system with feedback.

11. Define the input resistance with feedback for voltage series feedback amplifier?
a) $R_{IF} = (1\text{-}AB)$
b) $R_{IF} = (AB\text{-}1)$

c) $R_{IF} = (1+AB)$
d) None of the mentioned
Answer: c
Explanation: In feedback amplifier, the input resistance of the op-amp with feedback is (1+AB) times that of without feedback.

12. When the non-inverting input terminal of an op-amp is equal to that of the inverting input terminal (ideally)
a) $a \to \infty$
b) $V_{id} \cong 0$
c) $A_F = 1+(R_F / R_1)$
d) All of the mentioned
Answer: d
Explanation: When the input at both the terminal are equal, the difference input voltage, $V_{id} = V_{in1} - V_{in2}$.
=> $V_{id} \cong 0$ ($\because V_{in1} = V_{in2}$)
The open loop voltage gain, $A = V_o / V_{id} = V_o/0 = \infty$ and
the closed loop voltage gain, $A_F = V_o / V_{in} = 1 + (R_F / R_1)$

13. Find the input and output resistance for the circuit shown.
Specification for 741 op-amp : A=400000 ; $R_i = 33M\Omega$; $R_o = 60\Omega$;
$R_F = 11k\Omega$; $R_1 = 2k\Omega$; Supply voltage = ± 15v; Maximum output voltage swing = ± 13v.



a) $R_{IF} = 66M\Omega$, $R_{OF} = 30\Omega$
b) $R_{IF} = 30M\Omega$, $R_{OF} = 6k\Omega$
c) $R_{IF} = 15k\Omega$, $R_{OF} = 50M\Omega$
d) None of the mentioned
Answer: a
Explanation: $A_F = 1+(R_F/R_1) = 1+(11k\Omega/2k\Omega) = 6.5$;
$B = 1/ A_F = 1/6.5 = 0.154$;

Input resistance of $R_{IF} = R_1(1+AB) = 33M\Omega[1+(6.5*0.154)] = 66M\Omega$;
Output resistance of $R_{OF} = R_o/(1+AB) = 60/[1+(6.5*0.154)] = 29.98 \cong 30\Omega$.

14. The output resistance of the op-amp with feedback is
a) Same as that of the output resistance without feedback
b) Greater than that of the output resistance without feedback
c) Smaller than that of the output resistance without feedback
d) None of the mentioned
Answer: c
Explanation: In voltage series feedback amplifier, the output resistance is (1/(1+AB)) times the output resistance of the op-amp. Therefore, the output resistance of the op-amp with feedback is much smaller than the output resistance without feedback.

15. Find the output current in the voltage series feedback amplifier.
a) $i_o = \{[V_o+(A*V_{id})]/R_o\}$
b) $i_o = \{[V_o-(A*V_{id})]/R_o\}$
c) $i_o = (V_o/R_o)*A$
d) $i_o = [A*(V_o-V_{id})]/R_o$
Answer: b
Explanation: The output current in voltage series feedback amplifier is given as $i_o = \{[V_o-(A*V_{id})]/R_o\}$.

16. Find the unity gain bandwidth for voltage series feedback amplifier?
a) UBG = Af_o
b) UBG = Af_F
c) UBG = $Af_o\, f_F$
d) UBG = $A_F f_o$
Answer: a
Explanation: The unity gain bandwidth is given as product of open loop voltage gain and break frequency of an op-amp.

17. The bandwidth of a non-inverting amplifier with feedback is equal to
a) $f_o(AB)$
b) $f_o(AB-1)$
c) $f_o(1+AB)$
d) $f_o(1-AB)$
Answer: c
Explanation: The bandwidth of the non-inverting amplifier with feedback is equal to its bandwidth without feedback times (1+AB). i.e. $f_F=f_o(1+AB)$.

18. How are the saturation voltage specified on the manufacture's datasheet?
a) Negative voltage
b) Output voltage swing
c) Supply voltage
d) None of the mentioned
Answer: b

Explanation: In an open loop op-amp, the total output offset voltage (i.e. output voltage swing) is equal to either the positive or negative saturation voltage.

19. What is the formula for total output offset voltage with feedback?
a) $V_{ooT} = \pm V_o/(1+AB)$
b) $V_{ooT} = \pm V_{sat}*(1+AB)$
c) $V_{ooT} = \pm V_{sat}/(1+AB)$
d) $V_{ooT} = \pm V_o*(1+AB)$
Answer: c
Explanation: The total output offset voltage with feedback = (Total output offset voltage witput feedback) / (1+AB). i.e. $V_{ooT} = \pm V_{sat}/(1+AB)$.

20. Which of the following has the same characteristic as that of non-inverting amplifier with feedback?
a) Perfect feedback amplifier
b) Voltage follower
c) Perfect voltage amplifier
d) All of the mentioned
Answer: c
Explanation: A perfect voltage amplifier has very high input resistance, very low output resistance, stable voltage gain, large bandwidth and very little output offset voltage.
From the analysis of the characteristic of non-inverting amplifier with feedback, it is clear that it exhibits the characteristics of a perfect voltage amplifier.

21. What is the gain of voltage follower?
a) Gain > ∞
b) Gain –>1
c) Gain <1
d) Gain –>∞
Answer: b
Explanation: Voltage follower is non-inverting amplifier configured for unity gain. Such that the output voltage is equal to and in phase with the input.

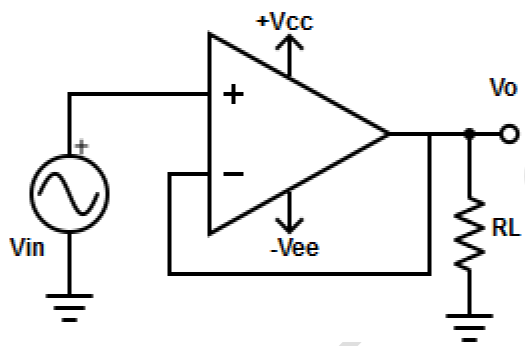
22. Which is preferred to attain higher input resistance and the output amplitude equal to input?
a) Voltage follower
b) Voltage series feedback amplifier
c) Voltage shunt feedback amplifier
d) Inverter
Answer: a
Explanation: In the voltage follower the output follow the input due to unity gain. Therefore, it is attained to get higher input resistance and output amplitude equal to input.

23. Find the input and output voltage in voltage follower circuit?
a) V_{in}=2v and V_{out} = 3v
b) V_{in}=10v and V_{out} = 11v
c) V_{in}=9v and V_{out} = 9v

d) V_{in}=4v and V_{out} = 7v
Answer: c
Explanation: Voltage follower has input voltage equal to output voltage. The closed loop voltage gain is equal to one. For example, take the input and output voltage to be 2v, then $A_F = V_{out}/V_{in}$ = 2v/2v = 1.

24. Voltage follower is also called as
a) None of the mentioned
b) Non-inverting amplifier
c) Inverting amplifier
d) Normal buffer
Answer: b
Explanation: The voltage follower is also called as a non-inverting buffer because, when placed between two networks, it removes the loading on the first network.

25. Find the bandwidth and total output offset voltage of a voltage follower? The following are the specifications for the op-amp 741: A=200000, f_o =5hz and supply voltage =±15v.



a) f_F = 1000hz, V_{ooT} = ± 7.5µv.
b) f_F = 100khz, V_{ooT} = ± 7.5µv.
c) f_F = 10khz, V_{ooT} = ±7.5µv.
d) f_F = 1000khz, V_{ooT} = ± 7.5µv.
Answer: d
Explanation: Bandwidth f_F =A* f_F = 200000*5= 1Mhz.
Total output offset voltage, V_{ooT}= ±V_{sat}/A= ±15/200000 =± 7.5µv

Voltage Shunt Feedback Amplifier

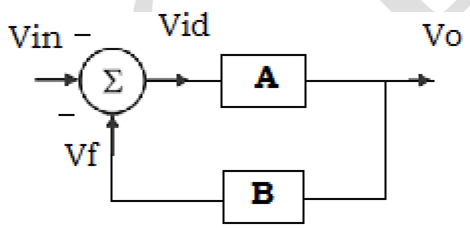
1. Voltage shunt feedback amplifier forms
a) A negative feedback
b) A positive feedback
c) Both positive and negative
d) None of the mentioned
Answer: a
Explanation: A voltage shunt feedback amplifier forms a negative feedback because, any increase in the output signal results in a feedback signal into the inverting input causing a decrease in the output signal.

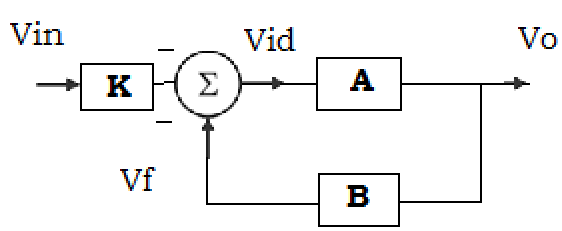
2. The value of feedback resistor and resistor connected in series with the input signal source are equal to 10kΩ and 3.3kΩ. Calculate the closed loop voltage gain?
a) -6.7
b) -33
c) -13.3
d) -3.33
Answer: d
Explanation: Closed loop voltage gain, $A_F = -R_F/R_1 = -10k\Omega/3.3k\Omega = -3.33$.

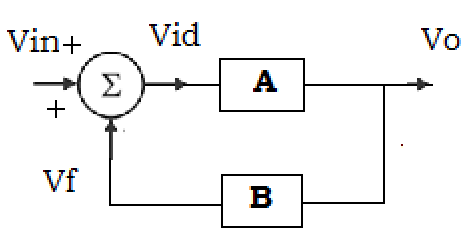
3. Write the formula for closed loop voltage gain of inverting amplifier with feedback using open loop voltage gain and gain of feedback circuit.
a) $A_F= A/(1+AB)$
b) $A_F= -A/(1+AB)$
c) $A_F= -B/(1+AB)$
d) None of the mentioned
Answer: c
Explanation: The closed loop voltage gain of the amplifier is $A_F= -Ak/(1+AB)$, where k is a voltage attenuation factor. In addition to phase inversion, A_F is k times the closed loop gain of the non-inverting amplifier where $k<1$.

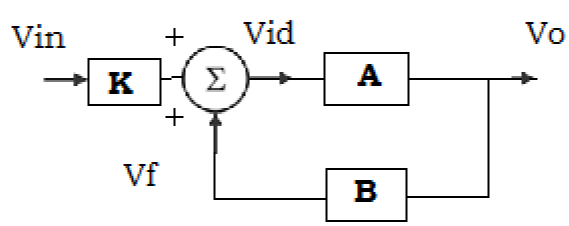
4. Voltage shunt feedback amplifiers are also called as
a) Non-inverting amplifier with feedback
b) Non-inverting amplifier without feedback
c) Inverting amplifier with feedback
d) Inverting amplifier without feedback
Answer: c
Explanation: The input and output signal in voltage series feedback amplifier are 180° out of phase (or of opposite polarities). Due to this phase inversion, the configuration is also called as inverting amplifier with feedback.

5. Find the block diagram representation for inverting amplifier with feedback

a)


b)


c)


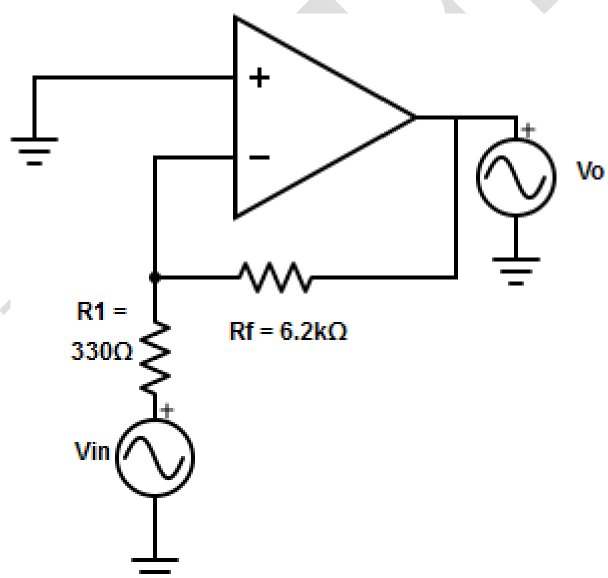
d)


Answer: b
Explanation: The block diagram of non-inverting amplifier is identical to that of inverting amplifier except for the voltage attenuation factor or block. However, the major difference is that a voltage summing junction is being used as a model for what is actually a current summing.

6. The inverting input inverting of the voltage shunt feedback resistor is a commonly named as
a) Terminal ground
b) Virtual ground
c) Virtual input
d) Resistive input
Answer: b
Explanation: Ideally, the difference between input voltages is zero. Therefore, the voltage at the inverting terminal is approximately equal to that of non-inverting terminal. In other words, the inverting terminal voltage is approximately at ground potential and it is said to be virtual ground.

7. Compute R_{IF} for an inverting amplifier with feedback, where the value of input resistance of op-amp is 4.7kΩ.
a) 4.7kΩ
b) 9.4kΩ
c) 2.35kΩ
d) Data given is insufficient
Answer: a
Explanation: In voltage shunt feedback amplifier, the input resistance with feedback is given as $R_{IF} = R_1$ (ideally).

8. Specification of op-amp 741c is given below:
A=200000; R_i=2MΩ; R_o=75Ω; Supply voltages= ±15v; output voltage swing =±13v; f_o=5hz.



Compute the value of output resistance, bandwidth and closed loop voltage gain for the circuit shown.

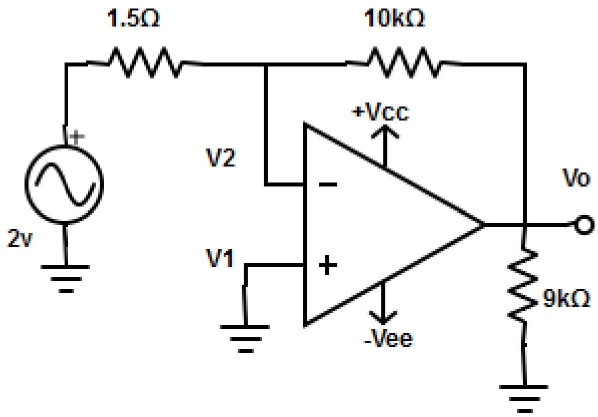
a) R_{OF}=8.6mΩ , f_F= 53005hz and A_F=-9.36
b) R_{OF}=4.12mΩ , f_F= 53005hz and A_F=-11.78
c) R_{OF}=7.1mΩ , f_F = 53005hz and A_F=-16.95
d) R_{OF}=1.9mΩ , f_F= 53005hz and A_F=-10
Answer: c
Explanation: Output resistance of the amplifier, R_{OF}= R_o/(1+AB) =, where B= R_1+R_F = 330Ω/330Ω+6.2kΩ = 0.053.
=> R_{OF}= ±75/(1+200000*0.053) = 53005hz.
Closed loop voltage gain, A_F= -(A*K)/(1+AB), Where k= R_F/(R_1+$_F$) = 6.2kΩ/(330Ω+6.2kΩ) = 0.949
=> A_F = -(200000*0.949)/[1+(200000*0.0535)] = -16.95.

9. What is the break frequency of the op-amp?
a) f_o = Unity Gain Bandwidth /closed loop voltage gain
b) f_o = Unity Gain Bandwidth / open loop voltage gain
c) f_o = Unity Gain Bandwidth /Gain of feedback circuit
d) All of the mentioned
Answer: c
Explanation: The mentioned formula is the general break frequency of any operational amplifier.

10. The total voltage offset voltage with feedback (V_{ooT}) equation for inverting amplifier is
a) Same as that of non-inverting amplifier
b) k times the non-inverting amplifier, k-> voltage attenuation factor
c) Twice the equation of non-inverting amplifier
d) All of the mentioned
Answer: a
Explanation: V_{oot} equation for inverting amplifier is the same as that of the non-inverting amplifier because, when the input signal is reduced to zero, both inverting and non-inverting amplifier results in the same circuit.

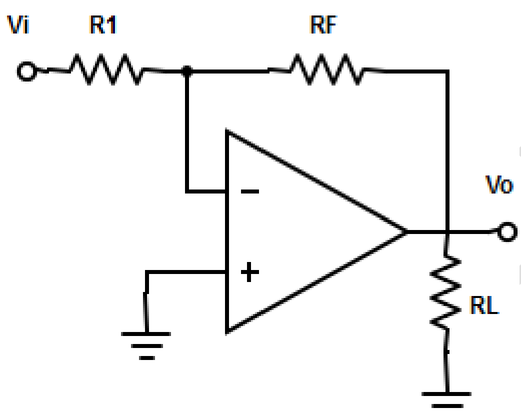
11. Which among the following is not a special case of voltage shut feedback amplifier?
a) Voltage follower
b) Current to voltage connector
c) Inverter
d) None of the mentioned
Answer: a
Explanation: A voltage follower is a special case of non-inverting amplifier (or voltage series feedback amplifier) and it has a gain of unity.

12. Compute the output voltage for the given circuit



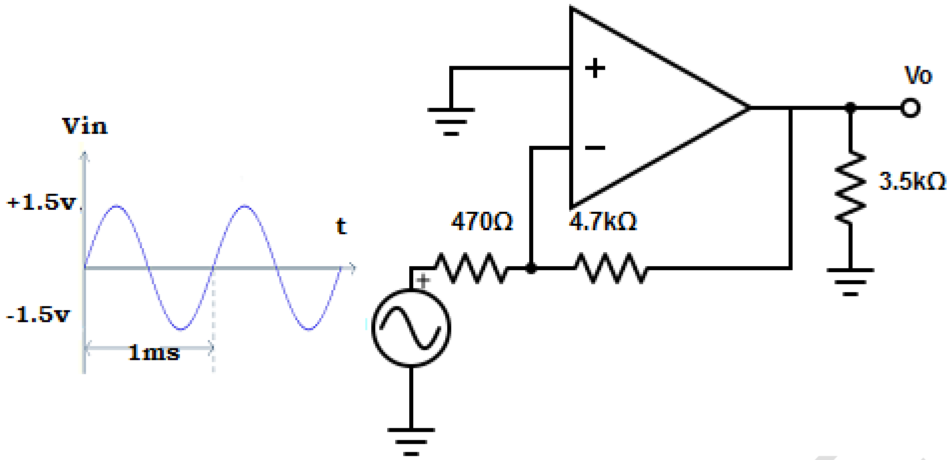
a) -2.6v
b) -27.8v
c) -26.7v
d) -0.267v
Answer: c
Explanation: The given circuit is a current to voltage converter. Since V_1 =0v and V_1= V_2.
=> i_{in} = V_{in}/R_1 = 4/ 1.5kΩ =2.67mA.
The output voltage V_o = $-i_{in}*R_F$ = -2.67mA*10kΩ = -26.7v.

13. At what condition an inverting amplifier works as an inverter

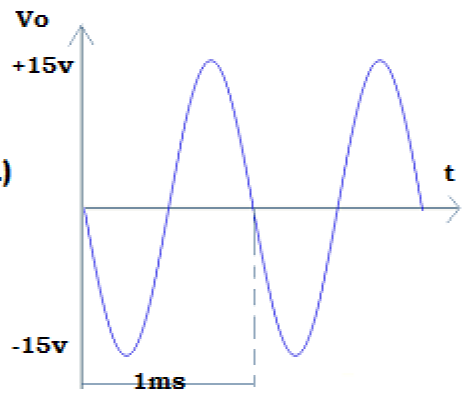


a) $R_1 = R_F + R_L$
b) $R_F = (R_1 * V_{in})/R_L$
c) $R_1 = R_F$
d) $R_1 = V_o/(V_{in} * R_L)$
Answer: c
Explanation: If $R_1 = R_F$, the inverting amplifier will work as an inverter.

14. Determine the output waveform for the given input signal



a)



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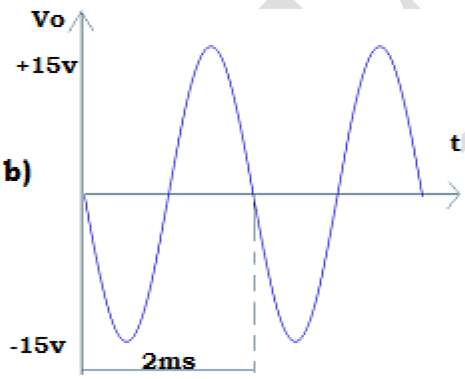

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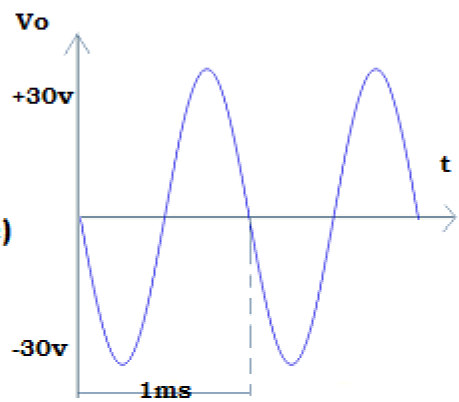

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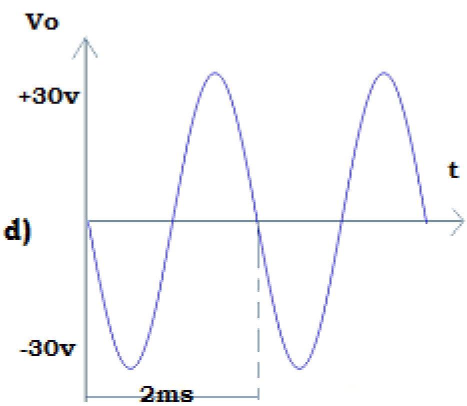
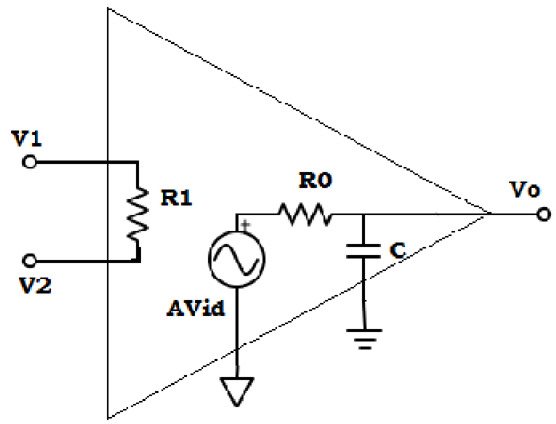


Answer: a
Explanation: Given, V_{in}= 3Vpp sinewave at 1khz (Therefore F=1/T=1/ms =1khz)
=> i_{in}= V_{in}/R_1 = 3/ 470=6.4mA
=> V_o=- i_{in}*R_F=6.4mA*4.7kΩ = 30 Vpp sinewave at 1khz.

Open-Loop Voltage Gain as a Function of Frequency

1. Determine the output voltage for an op-amp with single break frequency.



a) $V_O =\{ jX_C /[R_o+(iX_C)]\} \times AV_{id}$
b) $V_O = = AV_{id} / [1+j2\pi fR_oC]$.
c) $V_O = AV_{id} /(R_o+j2\pi fC)$
d) $V_O = V_{id} / [R_o-(j2\pi fR_oC)]$.
Answer: b
Explanation: The output voltage for an op-amp with single break frequency,
$V_O = \{(-jX_C) / [(R_o)-(jX_C)\} \times AV_{id}$
$\because$ $-j=1/j$ & $X_C =1/2\pi fC$
=> $V_O = \{(1/j2\Pi fC)/[R_o + (1/ j2\pi fC)] \} \times AV_{id} = AV_{id} / [1+ j2\pi fR_oC]$.

2. Compute the break frequency of an op-amp, if the output resistance=10kΩ and capacitor connected to the output =0.1μF.
a) 159.2Hz
b) 6.28Hz
c) 318.4Hz
d) 1000Hz
Answer: a
Explanation: Break frequency of the op-amp is given as $f_o = 1/(2\pi R_oC)= 1/ (2\pi\times 10k\Omega\times 0.1\mu F) = 1/ (6.28\times 10^{-3}) = 159.2Hz$.

3. The open loop voltage gain as a function of frequency is defined as
a) $A_{OL}(f) = V_O/V_{in}$
b) $A_{OL}(f) = V_O/V_{id}$
c) $A_{OL}(f) = V_O/V_f$
d) All of the mentioned
Answer: b
Explanation: The open loop voltage gain as a function of frequency is defined as ratio of output voltage to the difference of input voltages.

4. Which among the following factor remain fixed for an op-amp?
a) Open loop voltage gain

b) Gain of the op-amp
c) Operating frequency
d) Break frequency of the op-amp
Answer: d
Explanation: Break frequency f_o depends on the value of capacitors and on output resistance. Therefore, f_o is fixed for any op-amp.

5. Find the gain magnitude and phase angle of the op-amp using the specifications:
f= 50Hz; f_o=5Hz ; A=140000.
a) $A_{OL}(f)$= 22.92dB , $\Phi(f) = -89.99^o$
b) $A_{OL}(f)$= 66dB , $\Phi(f) = -90^o$
c) $A_{OL}(f)$= 26dB, $\Phi(f) = -89.99^o$
d) $A_{OL}(f)$= 20dB , $\Phi(f) = -84.29^o$
Answer: a
Explanation: The open loop gain magnitude $|A_{OL}(f)|= 20\log[A/\sqrt{[1+ f/f_o)^2}] = 20\log A-20 \log[A/\sqrt{[1+(f/f_o)^2}] = 20\log(140000)- 20\log[\sqrt{(1+(50,000/5)^2)}]$ $A_{OL}(f)$ dB= 102.922-80 = 22.92dB.
Phase angle, $\varphi(f) = -\tan^{-1}(f/f_o) = -\tan^{-1}(50000/5) = -89.99^o$.

6. Consider an op-amp where the inverting input voltage =3.7mv, non-inverting input voltage=6.25mv and open loop voltage gain =142dB. Find the output voltage.
a) 0.21v
b) 0.45v
c) 0.78v
d) 0.36v
Answer: d
Explanation: Open loop voltage gain, $A_{oL}(f) = V_o/V_{id}$
$V_O = A_{OL}(f) \times (V_{in1}-V_{in2})$ = 142 dB×(6.25-3.7) = 142×2.55 = 0.36v.

7. Express the open loop gain of the op-amp in complex form?
a) $A/\sqrt{[1+(f/f_o)^2}$
b) $20\log\{A/\sqrt{[1+(f/f_o)^2}\}$
c) $A/[1+j(f/f_o)]$.
d) None of the mentioned
Answer: c
Explanation: The open loop gain of the op-amp $A_{OL}(f)$ is a complex quantity and is expressed as $A_{OL}(f) = A/[1+ j(f/f_o)]$. The remaining equations are expressed in polar form.

8. Determine the difference between two $A_{OL}(f)$ at 50Hz and 500Hz frequency? (Consider the op-amp to be 741c)
a) 40dB
b) 30dB
c) 20dB
d) 10dB
Answer: c
Explanation: $A_{OL}(f)$ dB= $20\log[\sqrt{[1+ (f/f_o)^2}]$ At f= 50 Hz,
$A_{OL}(f)$ dB = $20\log(200000)- 20\log(\sqrt{(1+(50/5)^2})$ = 106.02-20.04 ≅ 86dB

At f= 500Hz
$A_{OL}(f)$ dB =20log(200000)-20log($\sqrt{(1+(500/5)^2}$) = 106.02-40 ≅ 66dB
Therefore, the difference between $A_{OL}(f)$dB = 86-66 = 20dB.

9. At what frequency, the phase shift between input &output voltage will be zero?
a) -40Hz
b) 0Hz
c) -22Hz
D) 20Hz
Answer: b
Explanation: At 0Hz the phase shift between input and output voltage is zero.
At f=0Hz, $\varphi(f) = -\tan^{-1}(f/f_o) = -\tan^{-1}(0/5) = 0^o$

10. At what frequency $A_{OL}(f)$=A?
a) 50Hz
b) 10Hz
c) 5Hz
d) 0Hz
Answer: d
Explanation: For any frequency less than break frequency (f_o =5Hz) the gain is approximately constant and is equal to A. For example, f_o =0Hz,
Then $A_{OL}(f)$ dB= 20log(200000-20log[$\sqrt{1+(0/5)^2}$)] = 106dB. Where A =20,000 ≅ 106dB.

11. What happen when the frequency increases?
a) $A_{OL}(f)$ continues to drop
b) A increases
c) f_o –> 0Hz
d) None of the mentioned
Answer: a
Explanation: The open loop voltage gain as a function of frequency is given as $A_{OL}(f) = A/ [\sqrt{1+} (f/f_o)]$ at frequency above f_o, the denominator value increases, causing the gain, $A_{OL}(f)$ to decrease. Thus, as frequency increases, the gain $A_{OL}(f)$ continuous to drop.

12. What will be the absolute value of phase shift, if the frequency keeps increasing?
a) Increase towards 45^o
b) Decrease towards 45^o
c) Increase towards 90^o
d) Decrease towards 90^o
Answer: c
Explanation: For any frequency above break frequency, the absolute value of phase shift increases towards 90^o with increase in frequency.

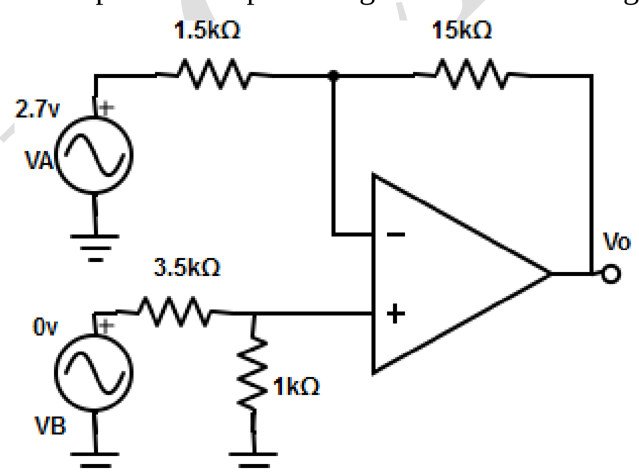
Differential Amplifiers with Multiple Op-Amp

1. Why differential amplifiers are preferred for instrumentation and industrial applications?
a) Input resistance is low
b) Produce amplified output
c) Amplify individual input voltage
d) Reject common mode voltage
Answer: d
Explanation: Differential amplifiers are preferred in these applications because they are better able to reject common-mode voltage than single input circuits and present balanced input impedance.

2. Which of the following is a combination of inverting and non-inverting amplifier?
a) Differential amplifier with one op-amp
b) Differential amplifier with two op-amps
c) Differential amplifier with three op-amps
d) Differential amplifier with four op-amps
Answer: a
Explanation: In differential amplifier with one op-amp both the inputs are connected to separate voltage source. So, if any one of the source is reduced to zero, differential amplifier acts as an inverting or non-inverting amplifier.

3. What will be the output voltage when V_x =0v?
(Where V_x –> inverting input terminal of differential amplifier with one op-amp)
a) $V_o = -(1+R_F/R_1)*V_1$
b) $V_o = -(1- R_F/ R_1)*V_1$
c) $V_o = (1+ R_F/ R_1)*V_1$
d) $V_o = (R_F/ R_1)*V_1$
Answer: c
Explanation: When V_x =0v, the configuration is a non-inverting amplifier.

4. Compute the output voltage from the following circuit diagram?

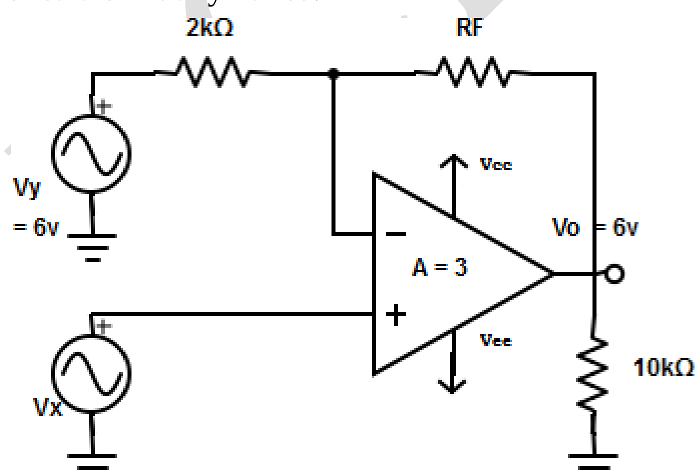


a) -17v
b) -27v
c) -39v
d) -15v
Answer: b
Explanation: Since V_B=0, the configuration becomes as an inverting amplifier. Hence, the output due to V_A is
$V_o = -(R_F/R_1)*V_A = -(15k\Omega/1.5k\Omega)*2.7v = -10*2.7 = -27v$.

5. Compute the output voltage if the input voltage is reduced to zero in differential amplifier with one op-amp?
a) Inverted Voltage
b) Same as the input voltage
c) Amplified inverted voltage
d) Cannot be determined
Answer: d
Explanation: It is not mentioned clearly whether inverting input or non-inverting input is reduced to zero. Therefore, the output cannot be determined.

6. The difference between the input and output voltage are -1v and 17v. Calculate the closed loop voltage gain of differential amplifier with one op-amp?
a) -51
b) 34
c) -17
d) 14
Answer: c
Explanation: Voltage gain of differential amplifier with one op-amp, A_D=Output voltage / Difference of input voltage
=> A_D = 17v/-1v = -17v.

7. For the differential amplifier given below, determine the V_x and R_F value. Assume that the circuit is initially nulled.



a) V_x = -8v, R_F = 9.9kΩ

b) V_x = 8v, R_F = 9.9kΩ
c) V_x = -8v, R_F = -9.9kΩ
d) V_x = 8v, R_F = -9.9kΩ
Answer: d
Explanation: The closed loop voltage gain, $A_D = -(R_F/R_1)$
=> RF = -3*3.3kΩ = -9.9kΩ
The net output is given is VO=-(RF /R1)*(Vx-Vy)
=> $V_x = V_y - V_o (-R_1 /R_F)$
=> V_x = 6+6(3.3kΩ/9.9kΩ) = 6+2 = 8v.

8. The gain of differential amplifier with one op-amp is same as that of
a) The inverting amplifier
b) The non-inverting amplifier
c) Both inverting and non-inverting amplifier
d) None of the mentioned
Answer: a
Explanation: The gain of differential amplifier is given as $A_D = -(R_F /R_1)$, which is equivalent to the output voltage obtained from the inverting amplifier.

9. Find the value of input resistance for differential amplifier with one op-amp. If $R_1 = R_2$=100Ω and $R_F = R_3$ =5kΩ.
a) R_{IFx} = 110Ω; R_{IFy} = 6.7kΩ
b) R_{IFx} = 100Ω; R_{IFy} = 5.1kΩ
c) R_{IFx} = 150Ω; R_{IFy} = 7.2kΩ
d) R_{IFx} = 190Ω; R_{IFy} = 9.0kΩ
Answer: b
Explanation: The input resistance of inverting amplifier is R_{IFx} = (R1) and the input resistance of non-inverting amplifier is R_{IFy} = (R2+ R3)
=> ∴ R_{IFx} = 100Ω and
=> R_{IFy} =100+5kΩ =5.1kΩ.

10. What is the net output voltage for differential amplifier with one op-amp
a) $V_o = -(R_F /R_1)*V_x$
b) $V_o = -(R_F /R_1)*(V_x-V_y)$
c) $V_o = (1+R_F /R_1)*(V_x-V_y)$
d) None of the mentioned
Answer: b
Explanation: The net output voltage for differential amplifier with one op-amp is given as $V_o= -(R_F /R_1)*(V_x-V_y)$

Slew Rate

1. Slew rate is defined as the rate of change of
a) Output voltage with respect to time
b) Input voltage with respect to time
c) Both output input voltage with respect to time

d) None of the mentioned
Answer: a
Explanation: Slew rate is the maximum rate of change of output voltage caused by a step input voltage with respect to time.

2. How the slew rate is represented?
a) 1V/ms
b) 1V/s
c) 1V/µs
d) 1mv/S
Answer: c
Explanation: Slew rate are usually specified in V/µs. For example, 1 V/µs means that the output rises or falls no faster than 1V every microsecond.

3. The natural semiconductor LH0063C has a slew rate of
a) 1400V/µs
b) 6000V/µs
c) 500V/µs
d) None of the mentioned
Answer: b
Explanation: National semiconductor LH0063C has a slew rate of 6000V/µs. Generally practical op-amp is available with slew rate from 0.1V/µs to well above 1000V/µs.

4. Rise time is specified for
a) Large signal
b) Medium signal
c) Small signal
d) All of the mentioned
Answer: c
Explanation: Rise time is specified for small signal, usually when the peak output voltage is less than one volt.

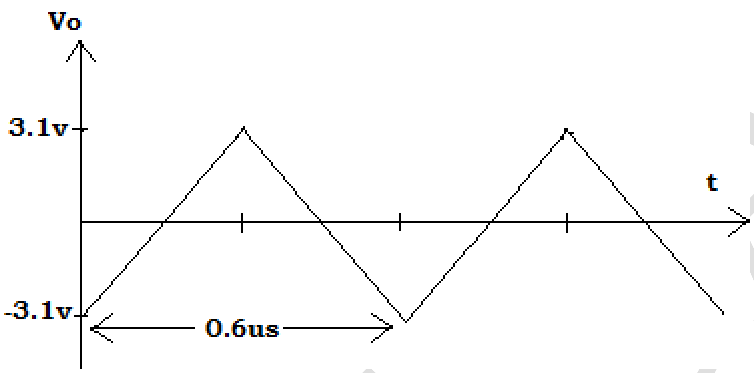
5. Op-amps with wide bandwidth will have
a) Increase in output
b) Higher slew rate
c) Low response time
d) None of the mentioned
Answer: b
Explanation: An op-amp slew rate is related to its frequency response. Usually op-amps with wider bandwidth have higher (better) slew rate.

6. Which factor is responsible for causing slew rate?
a) Internal capacitor
b) External resistor
c) None of the mentioned
d) Both internal and external capacitor

Answer: d
Explanation: Capacitors require a finite amount of time to charge and discharge. Thus, a capacitor inside or outside the op-amp causes slew rate.

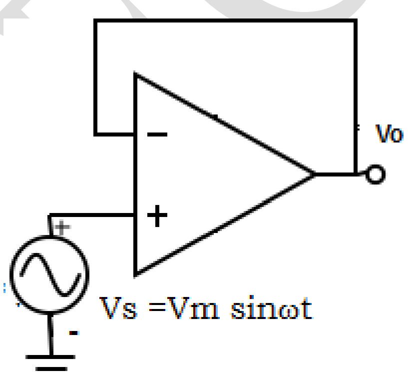
7. Find the value of capacitor, if the rate of change of voltage across the capacitor is 0.78V/µs and current= 12µA.
a) 5µF
b) 2µF
c) 10µF
d) 15µF
Answer: d
Explanation: Rate at which the voltage across the capacitor increases is given as $dV_c/dt = I/C$
=> $C = I/(dV_c/dt)$ = 12µA/0.78V/µs = 15.38 ≅15µF.

8. Find the slew rate of op-amp from the output waveform given below?



a) 3.4V/µs
b) 10V/µs
c) 20.66V/µs
d) 16V/µs
Answer: c
Explanation: Slew rate is defined as the maximum rate of change of the output
SR = 3.1-(-3.1v)/ (0.6/2)µs =6.3/0.3 = 20.66Vµs.

9. For the circuit shown below, calculate the rate of change of output signal



a) V_m ωcosωt

b) V_m cosωt
c) V_m cosωt/ωt
d) V_m cosωt/ω
Answer: a
Explanation: The given circuit is a voltage follower circuit. So, input voltage = output voltage
=> $V_o = V_m \sin\omega t$
=>∴ the rate of change of the output voltage = $dV_o/dt = d(V_m \sin\omega t)/dt = V_m \omega \cos\omega t$.

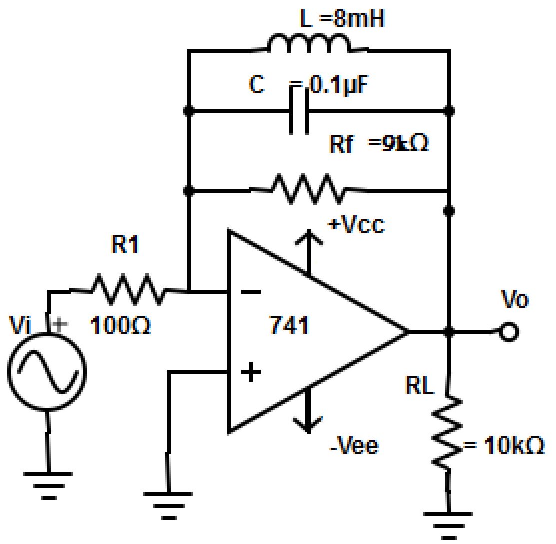
10. At what condition, the output of op-amp will be free of distortion?
a) Slew rate > $2\pi f V_m /10^6$ V/µs
b) Slew rate > $2\pi f V_m /10^6$ V/µs
c) Slew rate ≥ $2\pi f V_m /10^6$ V/µs
d) Slew rate = $2\pi f V_m /10^6$ V/µs
Answer: b
Explanation: As long as the value of right hand side equation is less than the slew rate of op-amp, the output wave form will always be undistorted.

Peak Amplifier

1. How the peaking response is obtained?
a) Using a series LC network with op-amp
b) Using a series RC network with op-amp
c) Using a parallel LC network with op-amp
d) Using a parallel RC network with op-amp
Answer: c
Explanation: The peaking response is the frequency response that peaks at a certain frequency. This can be obtained by using a parallel LC network with the op-amp.

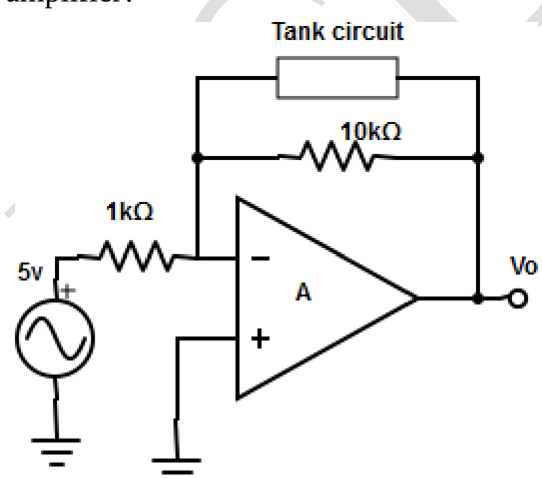
2. The expression for resonant frequency of the op-amp
a) $f_p = 1/[2\pi\times\sqrt{(LC)}]$.
b) $f_p = (2\pi\times\sqrt{L})/C$
c) $f_p = 2\pi\times\sqrt{(LC)}$
d) $f_p = 2\pi/\sqrt{(LC)}$
Answer: a
Explanation: The resonant frequency is also called as peak frequency, which is determined by the combination of L and C.
$f_p = 1/(2\pi\sqrt{LC})$.

3. From the circuit given below find the gain of the amplifier



a) 1.432
b) 9.342
c) 5.768
d) 7.407
Answer: d
Explanation: Frequency, f_p= 1/[2π×√(LC)] =1/[2π√(0.1µF×8mH)]=1/1.776×10^{-4}= 5.63kHz.
=> $X_L = 2\pi f_p L$ = 2π×5.63kHz×8mH = 282.85.
The figure of merit of coil, $Q_{coil}= X_L/R_1$= 282.85/100Ω = 2.8285.
∴ $R_p = (Q_{coil})^2 \times R_1$ = (2.8285^2)×100Ω= 800Ω.
The gain of the amplifier at resonance is maximum and given by
$A_F =-(R_F||R_p)/R_1$ = -(10kΩ||800)/100Ω =-740.740/100 = -7.407.

4. The parallel resistance of tank circuit and for the circuit is given below.Find the gain of the amplifier?



a) -778
b) -7.78
c) -72.8

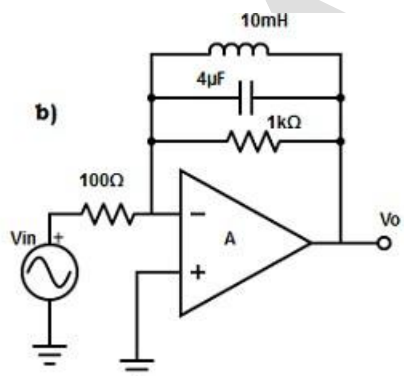
d) None of the mentioned
Answer: b
Explanation: The gain of the amplifier at resonance is the maximum and given by,
$A_F = -(R_F||R_p)/ R_1 = -[(R_p\times R_F)/ (R_F+R_p)] /R_1 = -[(10k\Omega\times 35k\Omega)/ (10k\Omega+35k\Omega)] /1k\Omega$
$\Rightarrow A_F = -\ 7.78k\Omega/1k\Omega = -7.78$.

5. The band width of the peaking amplifier is expressed as
a) $BW = (f_p\times X_L)/ (R_F+R_p)$
b) $BW = [f_p\times(R_F+R_p)\times X_L] / (R_F\times R_p)$
c) $BW = [f_p\times(R_F+R_p)] / (R_F\times R_p)$
d) $BW = [f_p\times(R_F+R_p)]/ X_L$
Answer: b
Explanation: The bandwidth of the peaking amplifier,
$BW = f_p/Q_p$, where Q_p – figure of merit of the parallel resonant circuit = $(R_f||R_p)/X_l = (R_f\times R_p)/[(R_f+R_p)\times X_l] \Rightarrow BW = [f_p\times(R_f+R_p)\times X_l] / (R_f\times R_p)$.

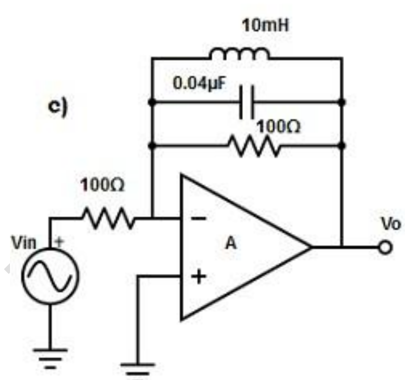
6. Design a peaking amplifier circuit to provide a gain of 10 at a peak frequency of 32khz given L=10mH having 30Ω resistance.

a) None of the mentioned

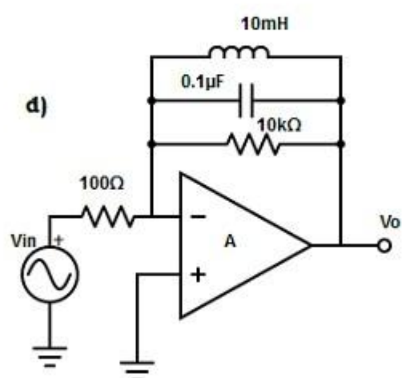
b)



c)



d)



Answer: b
Explanation: Given L=10mH and the internal resistance of the inductor R=30Ω. Assume R_1=100Ω. The gain times peak frequency= 10×32kHz=320kHz
$f_p = 1/2\pi\sqrt{LC}$
$\Rightarrow C = 1/[(2\pi)^2\times (f_p)^2\times L] = 1/ [(2\pi)^2\times(320)^2\times 10mH] = 1/252405.76 = 3.96\mu F \cong 4\mu F$.

$Q_{coil} = x_L/R = (2\pi f_p L)/R = (2\pi\times320kHz\times10mH)/30 = 20096/30 = 669.87$
$\Rightarrow R_p = (Q_{coil})^2\times R = (669.88)^2\times30 = 13.5M\Omega$
To find R_f,
$A_F = (R_F\times R_p)/[R_1\times(R_F+R_p)] \Rightarrow R_F = (A_f \times R_p \times R_1)/(R_p - A_F \times R_1)$
$R_F = (-10\times13.5\times10^6\times100) / (13.5\times10^6-(10\times100)) = 1000\Omega$
$\Rightarrow R_F = 1k\Omega$.
Thus the component values are $R_1=100\Omega$, $R_F= 1k\Omega$, L=10mH at R=30Ω and C = 4μF.

Instrumentation Amplifier

1. Strain gage is an example of which device?
a) Transducer
b) Voltage follower
c) Integrator
d) Differentiator
Answer: a
Explanation: Strain gage is a device when subjected to pressure or force undergoes change in its resistance.

2. An instrumentation system does not include
a) Transducer
b) Instrumentation amplifier
c) Automatic process controller
d) Tester
Answer: d
Explanation: Except tester the remaining blocks form the input, intermediate and output stage of instrumentation system.

3. Transmission line are used for
a) Output signal
b) Input signal
c) Signal transfer
d) All of the mentioned
Answer: c
Explanation: Transmission lines are the connecting line between the blocks and permits signal transfer from unit to unit.

4. The length of the transmission lines are
a) Longer than 10 meters
b) Shorter than 10 meters
c) Equals to 10 meters
d) None of the mentioned
Answer: d
Explanation: The length of the transmission lines depends primarily on the physical quantities being monitored and on system requirement.

5. Why output of transducer is not directly connected to indicator or display?
a) Low level output is produced
b) High level output is produced
c) No output is produced
d) Input is fed directly
Answer: a
Explanation: Many transducers do not produce output with sufficient strength to permit there use directly. Therefore, the low level output signal of transducer need to be amplified.

6. What are the features of instrumentation amplifier?
a) Low noise
b) High gain accuracy
c) Low thermal and time drift
d) All of the mentioned
Answer: d
Explanation: Instrumentation amplifiers are intended for precise low level signal amplification because of the features mentioned.

7. What is the disadvantage of using LH0036 instrumentation op-amp?
a) Extremely stable
b) Relatively expensive
c) Accurate
d) All of the mentioned
Answer:b
Explanation: LH0036 is a very precise special purpose circuit in which most electrical parameters are minimized and performance is optimized. So, it is relatively expensive.

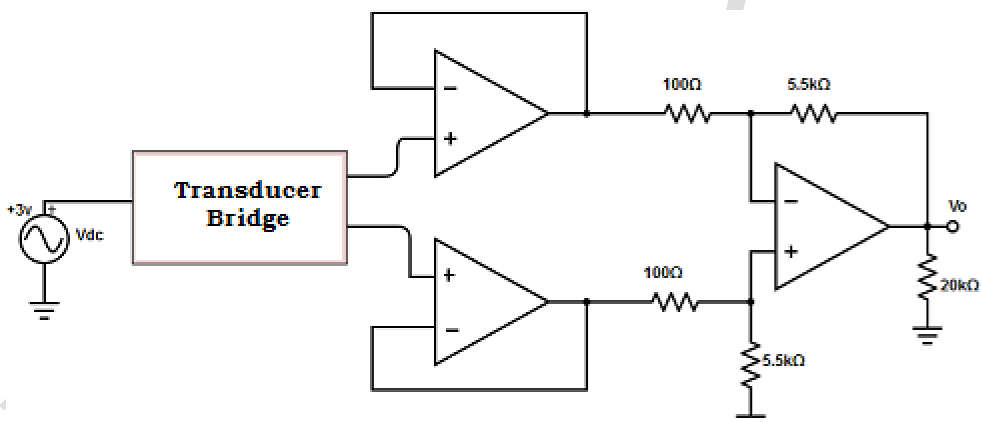
8. What instrument is used to amplify output signal of transducer
a) Peaking amplifier
b) Instrumentation amplifier
c) Differential amplifier
d) Bridge amplifier
Answer: b
Explanation: The major function of instrumentation amplifier is to amplify the low level output signal of the transducer, so that it can drive the output stages.

9. General purpose op-amps are used in applications as
a) Instrumentation amplifier
b) Differential instrumentation amplifier
c) Inverting instrumentation amplifier
d) Non-inverting instrumentation amplifier
Answer: b
Explanation: When the requirement for the application are not too strict. The general purpose op-amp can be employed in the differential mode. Such amplifiers are called as Differential instrumentation amplifier.

10. In an instrumentation amplifier using transducer bridge, which device measure the change in physical energy
a) Resistive transducer
b) Indicating meter
c) Capacitive transducer
d) Inductor circuit
Answer: a
Explanation: A resistive transducer is used to measure the change in same physical energy, which is connected to one arm of the bridge

11. The temperature of a thermistor increases, when the value of its resistance
a) Remain constant
b) Increase
c) Decrease
d) Depends on the heating material
Answer: c
Explanation: Thermistor is a semiconductor that behaves as resistor, with a negative temperature coefficient of resistance. As the temperature of thermistor increases, its resistance decreases.

12.



Consider the entire resistors in the bridge circuit are equal. The resistance and change in resistance are given as 3kΩ and 30kΩ. Calculate the output voltage of differential instrumentation amplifier?
a) 4.95v
b) 1.65v
c) 8.25v
d) 14.85v
Answer: b

Explanation: The output voltage of the circuit is $V_o = -(R_F/R_1)\times(\Delta R/R)\times V_{dc}$
$= (5.5k\Omega/100\Omega)\times(30k\Omega/3k\Omega)\times3 = 1.65v$.

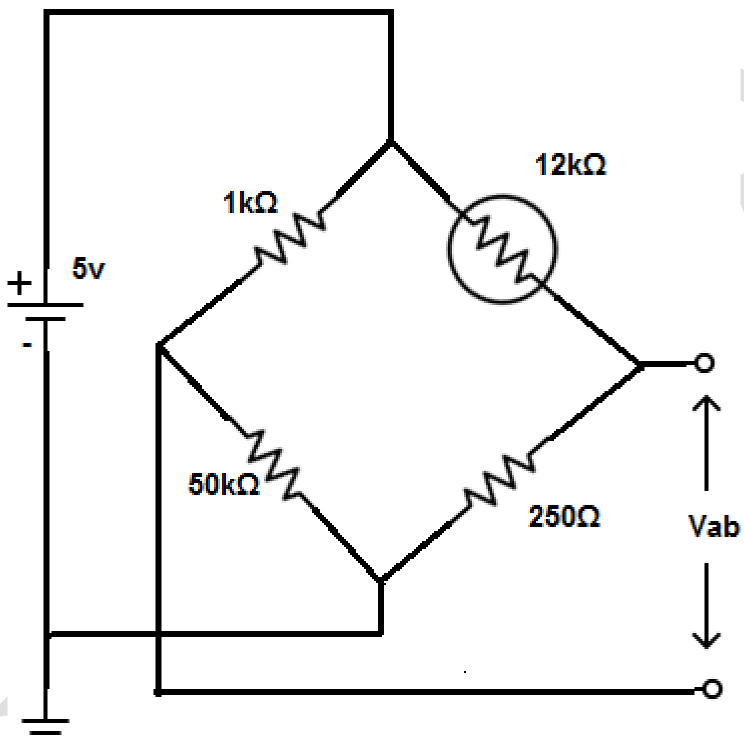
13. Consider a thermistor having the following specifications: R_F=150kΩ at a reference temperature of 35ºC and temperature coefficient of resistance = 25ºC. Determine the change in resistance at 100ºC.

a) -1.625MΩ
b) 9.75MΩ
c) 4.78MΩ
d) None of the mentioned

Answer: a

Explanation: Thermistor has negative temperature coefficient of resistance. Therefore, $\Delta R = -(25k\Omega/^{o}C)\times(100^{o}C-35^{o}C) = -1625k\Omega$.
$\Delta R = -1.625M\Omega$.

14. Consider the given bridge circuit, find the voltage across the output terminal, V_{ab}.



a) $V_{ab} = 4.9v$
b) $V_{ab} = -5.6v$
c) $V_{ab} = 1.2v$
d) $V_{ab} = -8.2v$

Answer: a

Explanation: According to the voltage divider rule,
$V_a = (R_a\times V_{dc})/[R_a+(R_T+\Delta R)] = (1k\Omega\times5v)/(1k\Omega+75k\Omega) = 0.065v$
$V_b = (R_b\times V_{dc})/(R_b+R_c) = (50k\Omega\times5v)/(50k\Omega+250\Omega) = 4.975v$
The voltage across the output terminal of the bridge, $V_{ab} = V_a - V_b = 4.9v$.

15. Express the equation for transducer bridge, if all the resistor values are equal
a) $v=-(\Delta R\times V_{dc})/(2\times R+\Delta R)$
b) $v=-(\Delta R\times V_{dc})/2\times(R+\Delta R)$
c) $v=-V_{dc}/[2\times(2\times R+\Delta R)]$.
d) $v=-(\Delta R\times V_{dc})/ [2\times(2\times R+\Delta R)]$.
Answer: d
Explanation: If the $R_a=R_b=R_c=R_T=R$(Equal), then the output voltage across the bridge terminals of the transducer bridge is $v=-(\Delta R\times V_{dc})/ [2\times(2\times R+\Delta R)]$.

16. Which type of thermistor is chosen for temperature measurement and control?
a) High temperature coefficient of resistance
b) Low temperature coefficient of resistance
c) Positive temperature coefficient of resistance
d) None of the mentioned
Answer: a
Explanation: Thermistors with a high temperature coefficient resistance are more sensitive to temperature change and are therefore well suited to temperature measurement and control.

17. Photo conductive cell changes it resistance with
a) Change in temperature
b) Material composition
c) Incident radiant energy
d) Change in elasticity
Answer: c
Explanation: Photoconductive cell is a type of transducer that changes its resistance or varies its resistance with an incident radiant energy with light.

18. What will be the resistance of a photoconductive cell in darkness?
a) 1000-3000Ω
b) 100MΩ
c) 250-500Ω
d) None of the mentioned
Answer: d
Explanation: The resistance of the photoconductive cell in darkness is typically in the order of 100kΩ.

19. Which material is used for photoconductive cells?
a) Germanium
b) Cadmium sulphide
c) Lithium
d) Phosphorous
Answer: b
Explanation: The conductivity in cadmium sulphide is a function of incident radiant energy. So, it is used for photoconductive cell.

20. Name the resistive transducer that varies its resistance on application of external stress?
a) Photocells
b) Light dependent
c) Stain gage
d) None of the mentioned
Answer: c
Explanation: Strain gage is a type of resistive transducer whose resistance changes due to elongation or compression when external stress is applied

21. Strain gage are used to monitor change in
a) Pressure
b) Torque
c) Displacement
d) All of the mentioned
Answer: d
Explanation: A strain gage may be used to monitor change in applied pressure, torque and displacement by measuring the corresponding change in the gage resistance.

22. Which type of resistive transducer is most commonly used?
a) Thermistor
b) Photoconductive cell
c) Strain gage
d) All of the mentioned
Answer: a
Explanation: Thermistors are most commonly used because they are relatively easy to mount.

23. What is the unit of strain gage?
a) $\Omega/^{o}C$
b) Lux
c) Newton / meter^2
d) Volts
Answer: c
Explanation: Strain gage changes resistance when an external stress is applied. Therefore, the stress is defined as force/unit area i.e. Newton / meter^2.

24. Which type of strain gage has better resolution?
a) Semiconductor strain gage
b) Wire strain gage
c) Wire and Semiconductor strain gage
d) None of the mentioned
Answer: a
Explanation: Semiconductor strain gage are much more sensitive than wire type and so, it provide better accuracy and resolution.

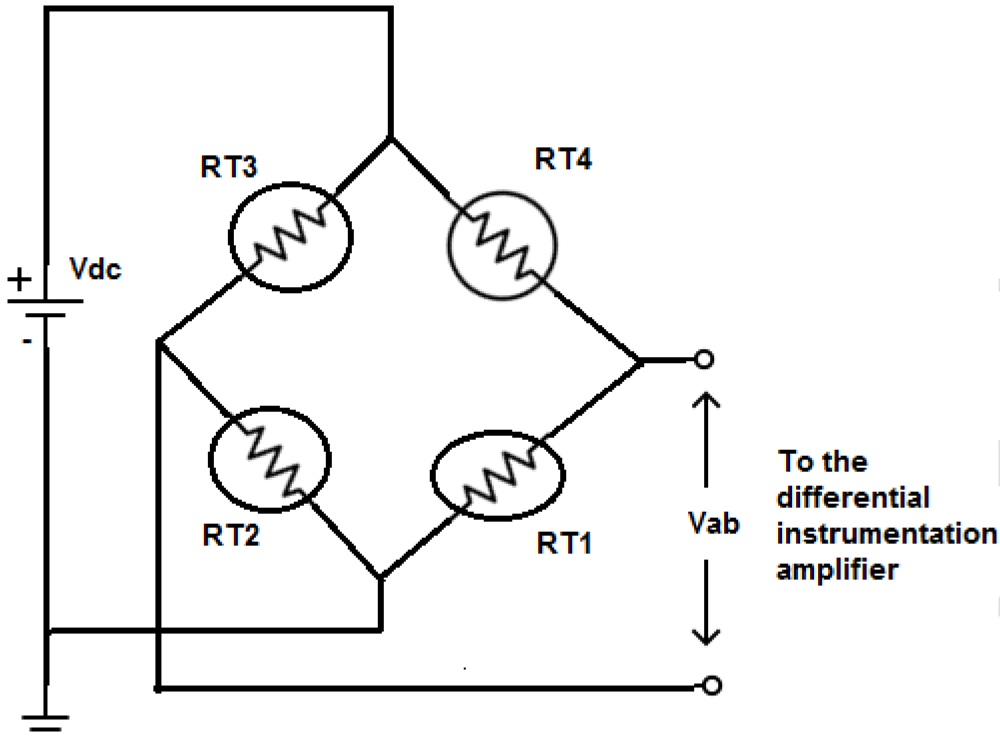
25. How a differential instrumentation amplifier using transducer bridge can be used as a temperature controller?

a) Increase room temperature
b) Replaces calibrated meter with relay
c) Change the bridge resistance
d) Replace thermistor by light intensity meter
Answer: b
Explanation: A simple and inexpensive temperature controller can be constructed by replacing a meter with a relay in the circuit. So, the output of the differential instrumentation amplifier drives a relay output of the differential instrumentation amplifier drives a relay that controls the current on the heat generating circuit.

26. The strain gage elements in the analog weight scale are mounted on a
a) Base of weight platform
b) Hanging weight platform
c) Loading weight platform
d) Varying weight platform
Answer: a
Explanation: The strain gage elements are mounted in the base of the weight platform. So, that whenever external force or weight is applied to the platform, one pair of element in the opposite arm of bridge elongates, whereas the other pair in opposite arm compresses.

27. What will be the resultant circuit, when the thermistor in the bridge transducer is replaced by a strain gage?
a) Differential input and differential output amplifier
b) Light intensity
c) Analog weight scale
d) None of the mentioned
Answer: c
Explanation: By connecting a strain gage in the transducer bridge, the differential instrumentation amplifier circuit can be converted in a simple and inexpensive analog weight scale.

28.



R_{T1}, R_{T2}, R_{T3}, R_{T4} are unstrained gage resistance. If the resistance change in each gage is 0.3Ω. Choose the correct option?

1. R_{T1} and R_{T3} increases by 0.3Ω
2. R_{T2} and R_{T4} decreases by 0.3Ω
3. R_{T1} and R_{T3} increases by 0.3Ω
4. R_{T2} and R_{T4} decreases by 0.3Ω

a) 3 and 4
b) 1 and 2
c) 1 and 4
d) 2 and 3

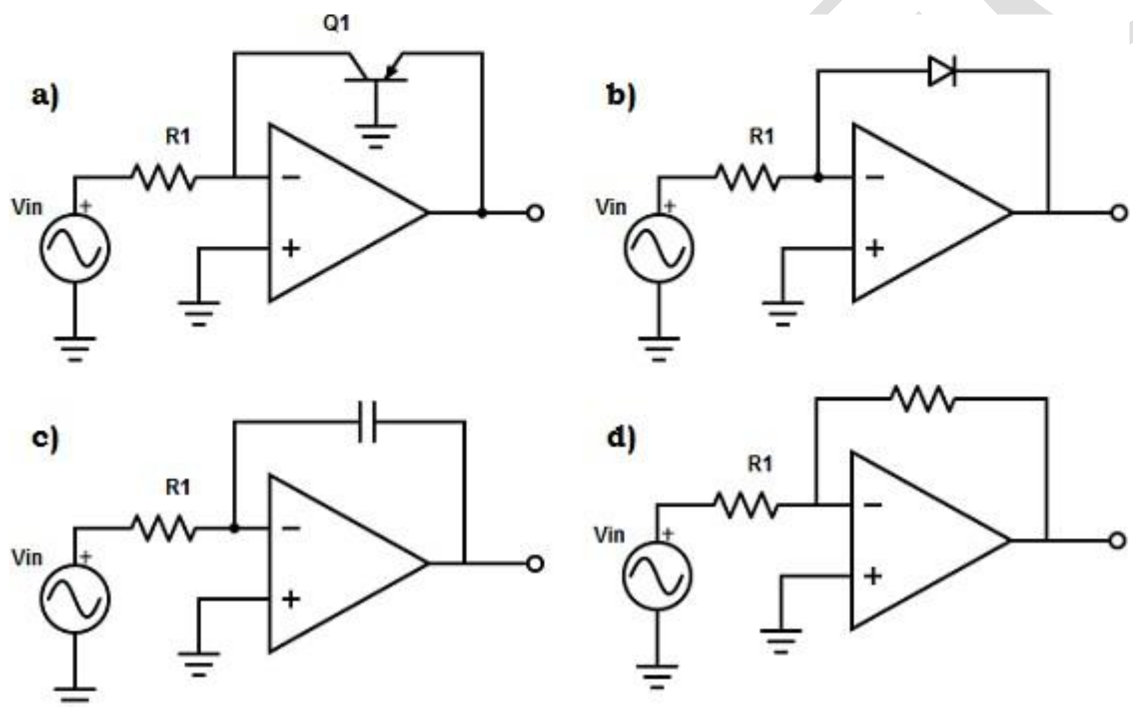
Answer: a

Explanation: When external weight is applied to the platform. One pair of element elongate and the other pair compresses. Therefore, R_{T1} and R_{T3} is ΔR and the increase in R_{T2} and R_{T4} is also by ΔR

Log and Antilog Amplifier

1. Which of the following functions does the antilog computation required to perform continuously with log-amps?
a) In(x)
b) log(x)
c) Sinh(x)
d) All of the mentioned
Answer: d
Explanation: Log-amp can easily perform function such as In(x), Log(x), Sinh(x) to have direct dB display on digital voltmeter and spectrum analyser.

2. Find the circuit that is used to compress the dynamic range of a signal?



Answer: a
Explanation: Log amps are used to compress the dynamic range of a signal. The fundamental log amp circuit consists of a grounded base transistor in the feedback path.

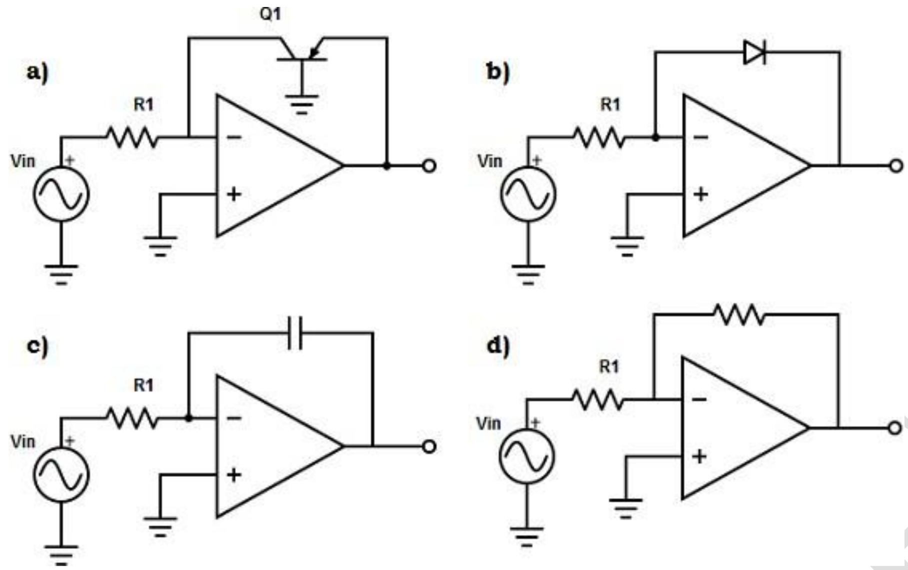
3. Find the output voltage of the log-amplifier
a) $V_O = -(kT)\times\ln(V_i/V_{ref})$
b) $V_O = -(kT/q)\times\ln(V_i/V_{ref})$
c) $V_O = -(kT/q)\times\ln(V_{ref}/V_i)$
d) $V_O = (kT/q)\times\ln(V_i/V_{ref})$
Answer: b
Explanation: the output voltage is proportional to the logarithm of input voltage.
$V_O = -(kT/q)\times\ln(V_i / V_{ref})$.

4. How to provide saturation current and temperature compensation in log-amp?
a) Applying reference voltage alone to two different log-amps
b) Applying input and reference voltage to same log-amps
c) Applying input and reference voltage to separate log-amps
d) None of the mentioned
Answer: c
Explanation: The emitter saturation current varies from transistor to transistor with temperature. Therefore, the input and reference voltage are applied to separate log-amps and two transistors are integrated close together in the same silicon wafer. This provides a close match of the saturation currents and ensures good thermal tracking.

5. The input voltage, 6v and reference voltage, 4 v are applied to a log-amp with saturation current and temperature compensation. Find the output voltage of the log-amp?
a) 6.314(kT/q)v
b) 0.597(kT/q)v
c) 0.405(kT/q)v
d) 1.214(kT/q)v
Answer: c
Explanation: The output voltage of saturation current and temperature compensation log-amp,
$V_O = (kT/q)\times\ln(V_i / V_{ref}) = (kT/q)\times\ln(6v/4v) = (kT/q)\times\ln(1.5)$
$V_O = 0.405(kT/q)v$.

6.Which of the following functions does the antilog computation required to perform continuously with log-amps?
a) In(x)
b) log(x)
c) Sinh(x)
d) All of the mentioned
Answer: d
Explanation: Log-amp can easily perform function such as In(x), Log(x), Sinh(x) to have direct dB display on digital voltmeter and spectrum analyser.

7. Find the circuit that is used to compress the dynamic range of a signal?



Answer: a
Explanation: Log amps are used to compress the dynamic range of a signal. The fundamental log amp circuit consists of a grounded base transistor in the feedback path.

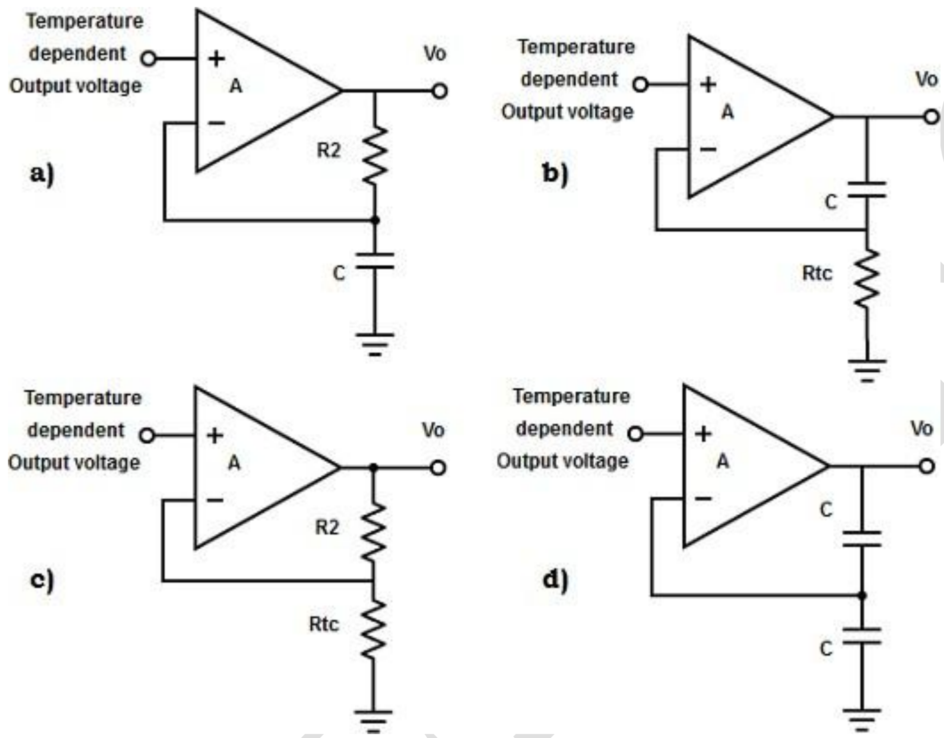
8. Find the output voltage of the log-amplifier
a) $V_O = -(kT)\times\ln(V_i/V_{ref})$
b) $V_O = -(kT/q)\times\ln(V_i/V_{ref})$
c) $V_O = -(kT/q)\times\ln(V_{ref}/V_i)$
d) $V_O = (kT/q)\times\ln(V_i/V_{ref})$
Answer: b
Explanation: the output voltage is proportional to the logarithm of input voltage.
$V_O = -(kT/q)\times\ln(V_i / V_{ref})$.

9. How to provide saturation current and temperature compensation in log-amp?
a) Applying reference voltage alone to two different log-amps
b) Applying input and reference voltage to same log-amps
c) Applying input and reference voltage to separate log-amps
d) None of the mentioned
Answer: c
Explanation: The emitter saturation current varies from transistor to transistor with temperature. Therefore, the input and reference voltage are applied to separate log-amps and two transistors are integrated close together in the same silicon wafer. This provides a close match of the saturation currents and ensures good thermal tracking.

10. The input voltage, 6v and reference voltage, 4 v are applied to a log-amp with saturation current and temperature compensation. Find the output voltage of the log-amp?
a) 6.314(kT/q)v
b) 0.597(kT/q)v
c) 0.405(kT/q)v

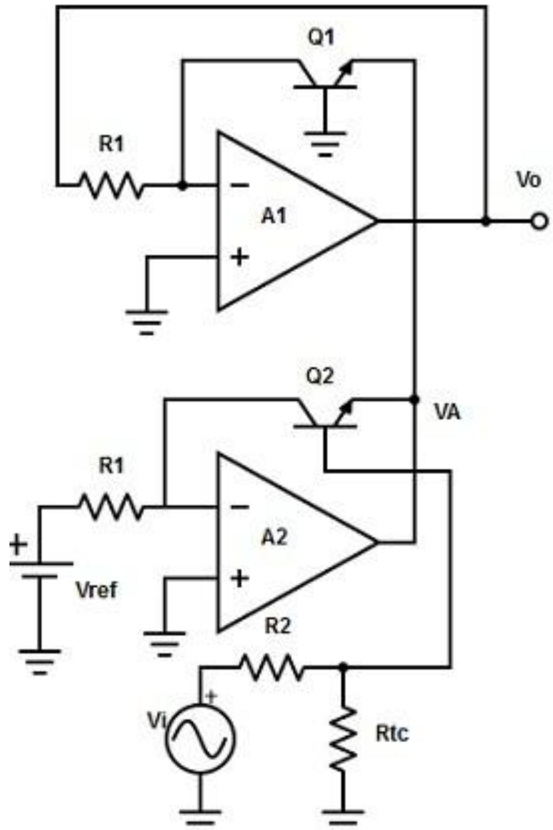
d) 1.214(kT/q)v
Answer: c
Explanation: The output voltage of saturation current and temperature compensation log-amp,
$V_O = (kT/q)\times\ln(V_i / V_{ref}) = (kT/q)\times\ln(6v/4v) = (kT/q)\times\ln(1.5)$
$V_O = 0.405(kT/q)v$.

11. Find the circuit used for compensating dependency of temperature in the output voltage?



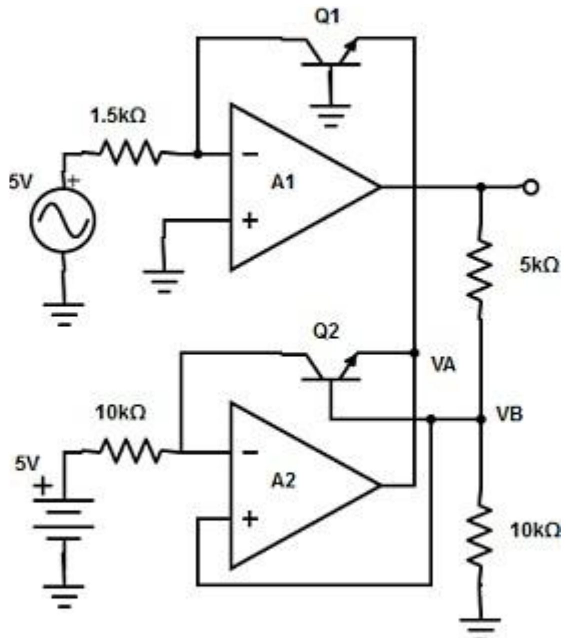
Answer: c
Explanation: The temperature dependence on the output voltage is compensated by connecting an op-amp which provide a non-inverting gain of $[1+ (R_2/ R_{TC})]$ at the output of the log-amp with saturation current compensation.
Now the output voltage becomes, $V_O = [1+ (R_2/ R_{TC})]\times[(kT/q)\times\ln(V_i / V_{ref})]$ Where, R_{TC} –> temperature sensitive resistance with a positive co-efficient of temperature.

12. Determine the output voltage for the given circuit



a) $V_O = V_{ref}/(10^{-k'v_i})$
b) $V_O = V_{ref}+(10^{-k'v_i})$
c) $V_O = V_{ref}\times(10^{-k'v_i})$
d) $V_O = V_{ref}-(10^{-k'v_i})$
Answer: c
Explanation: The output voltage of an antilog amp is given as, $V_O = V_{ref}\,(10^{-k'v_i})$
Where $k' = 0.4343\,(q/kt)\times[(R_{TC}/\,(R_2 + R_{TC})]$.

13. Calculate the base voltage of Q_2 transistor in the log-amp using two op-amps?



a) 8.7v
b) 5.3v
c) 3.3v
d) 6.2v
Answer: c
Explanation: The base voltage of Q_2 transistor, $V_B = [R_{TC} / (R_2 + R_{TC})] \times (V_i) = [10k\Omega/(5k\Omega+10k\Omega)] \times 5v = 3.33v$.

Multiplier and Divider

1. Determine output voltage of analog multiplier provided with two input signal V_x and V_y.
a) $V_o = (V_x \times V_x) / V_y$
b) $V_o = (V_x \times V_y / V_{ref}$
c) $V_o = (V_y \times V_y) / V_x$
d) $V_o = (V_x \times V_y) / V_{ref}^2$
Answer: b
Explanation: The output is the product of two inputs divided by a reference voltage in analog multiplier. Thus, the output voltage is a scaled version of x and y inputs.
=> $V_o = V_x \times V_y / V_{ref}$.

2. Match the list-I with list-II

List-I	List-II
1. One quadrant multiplier	i. Input 1- Positive, Input 2- Either positive or negative
2. Two quadrant	ii. Input 1- Positive, Input 2 – Positive

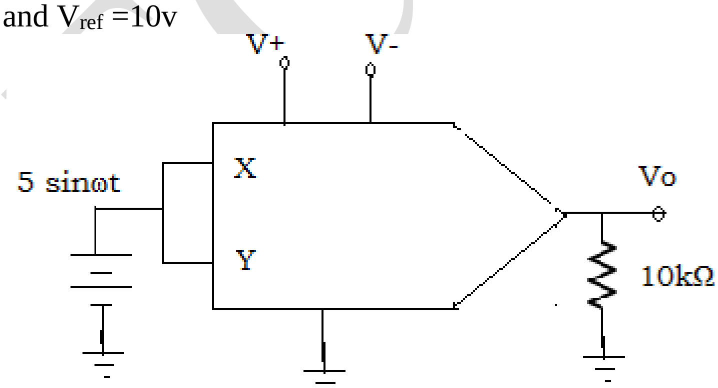
multiplier	
3. Four quadrant multiplier	iii. Input 1- Either positive or negative, Input 2- Either positive or negative

a) 1-ii, 2-i, 3-iii
b) 1-ii, 2-ii, 3-ii
c) 1-iii, 2-I, 3-ii
d) 1-I, 2-iii, 3-i
Answer: a
Explanation: If both inputs are positive, the IC is said to be a one quadrant multiplier. A two quadrant multiplier function properly, if one input is held positive and the other is allowed to swing. Similarly, for a four quadrant multiplier both the inputs are allowed to swing.

3. What is the disadvantage of log-antilog multiplier?
a) Provides four quadrant multiplication only
b) Provides one quadrant multiplication only
c) Provides two and four quadrant multiplication only
d) Provides one, two and four quadrant multiplication only
Answer: b
Explanation: Log amplifier requires the input and reference voltage to be of the same polarity. This restricts log-antilog multiplier to one quadrant operation.

4. An input of Vsinωt is applied to an ideal frequency doubler. Compute its output voltage?
a) $V_o = [(V_x \times V_y) / V_{ref}^2] \times [1-\cos2\omega t/2]$.
b) $V_o = [(V_x^2 \times V_y^2) / V_{ref}] \times [1-\cos2\omega t/2]$.
c) $V_o = [(V_x \times V_y)^2 / V_{ref}] \times [1-\cos2\omega t/2]$.
d) $V_o = [(V_x \times V_y) /(V_{ref}] \times [1-\cos2\omega t/2]$.
Answer: d
Explanation: In an ideal frequency doubler, same frequency is applied to both inputs.
$\therefore V_x = V_x\sin\omega t$ and $V_y = V_y\sin\omega t$
$\Rightarrow V_o = (V_x \times V_y \times \sin^2\omega t) / V_{ref} = [(V_x \times V_y) / V_{ref}] \times [1-\cos2\omega t/2]$.

5. Find the output voltage for the squarer circuit given below, choose input frequency as 10kHz and V_{ref} =10v



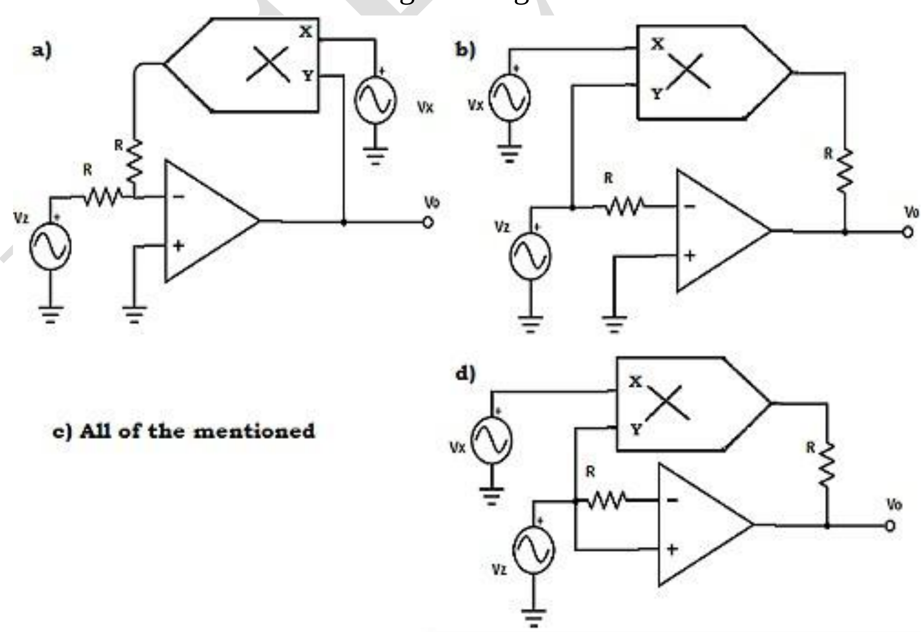
a) $V_o = 5.0-(5.0 \times \cos4\pi \times 10^4 t)$
b) $V_o = 2.75-(2.75 \times \cos4\pi \times 10^4 t)$

c) $V_o = 1.25-(1.25\times\cos4\pi\times10^4t)$
d) None of the mentioned
Answer: c
Explanation: Output voltage of frequency $V_o = V_i^2 / V_{ref}$
=> $V_i = 5\sin\omega t = 5\sin2\pi\times10^4t$
$V_o = [5\times(\sin2\pi\times10^4t)^2\,]/10 = 2.5\times[1/2-(1/2\cos2\pi\times2\times10^4t)] = 1.25-(1.25\times\cos4\pi\times10^4t)$.

6. Calculate the phase difference between two input signals applied to a multiplier, if the input signals are $V_x= 2\sin\omega t$ and $V_y= 4\sin(\omega t+\theta)$. (Take V_{ref}= 12v).
a) $\theta = 1.019$
b) $\theta = 30.626$
c) $\theta = 13.87$
d) $\theta = 45.667$
Answer: a
Explanation: $V_o= [V_{mx}\times V_{my}/(2\times V_{ref})]\times\cos\theta$
=> $(V_o\times2\times V_{ref})/(V_{mx}\times V_{my}) = \cos\theta$
=> $\cos\theta = (10\times2\times12)/(2\times4) = 30$.
=> $\theta = \cos^{-1}30 = 1.019$.

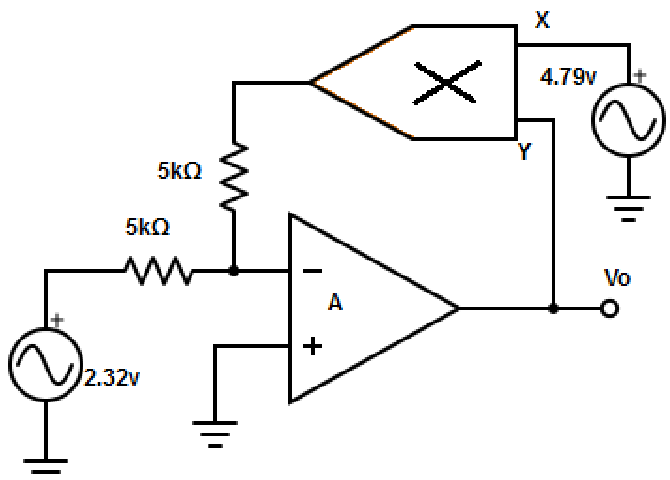
7. Express the output voltage equation of divider circuit
a) $V_o= -(V_{ref}/2)\times(V_z/V_x)$
b) $V_o= -(2\times V_{ref})\times(V_z/V_x)$
c) $V_o= -(V_{ref})\times(V_z/V_x)$
d) $V_o= -V_{ref}^2\times(V_z/V_x)$
Answer: c
Explanation: The output voltage of the divider, $V_o= -V_{ref}\times(V_z/V_x)$.
Where V_z –> dividend and V_x –> divisor.

8. Find the divider circuit configuration given below



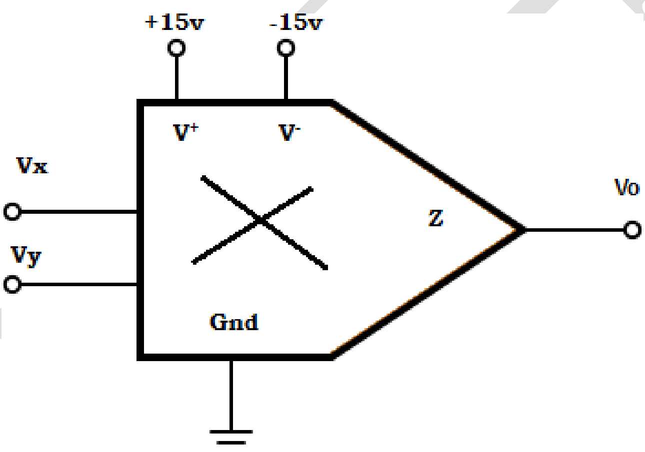
Answer: a
Explanation: Division is the complement of multiplication. So, the divider can be accomplished by placing the multiplier circuit element in the op-amp feedback loop.

9. Find the input current for the circuit given below.



a) $I_Z = 0.5372mA$
b) $I_Z = 1.581mA$
c) $I_Z = 2.436mA$
d) $I_Z = 9.347mA$
Answer: b
Explanation: Input current, $I_Z = -(V_x \times V_o)/(V_{ref} \times R) = -(4.79v \times 16.5v)/(10 \times 5k\Omega) = 1.581mA$.

10. Find the condition at which the output will not saturate?



a) $V_x > 10v$; $V_y > 10v$
b) $V_x < 10v$; $V_y > 10v$
c) $V_x < 10v$; $V_y < 10v$
d) $V_x > 10v$; $V_y < 10v$
Answer: c
Explanation: In an analog multiplier, V_{ref} is internally set to 10v. As long as $V_x < V_{ref}$ and $V_y < V_{ref}$, the output of multiplier will not saturate.

Integrator

1. The circuit in which the output voltage waveform is the integral of the input voltage waveform is called
a) Integrator
b) Differentiator
c) Phase shift oscillator
d) Square wave generator
Answer: a
Explanation: Integrator circuit produces the output voltage waveform as the integral of the input voltage waveform.

2. Find the output voltage of the integrator
a) $V_o = (1/R\times C_F)\times {}^t\int_0 V_{in}dt+C$
b) $V_o = (R/C_F)\times {}^t\int_0 V_{in}dt+C$
c) $V_o = (C_F/R)\times {}^t\int_0 V_{in}dt+C$
d) $V_o = (R\times C_F)\times {}^t\int_0 V_{in}dt+C$
Answer: a
Explanation: The output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant RC_F.
$V_o = (1/R\times C_F)\times {}^t\int_0 V_{in}dt+C$
Where C-> Integration constant and C_F-> Feedback capacitor.

3. Why an integrator cannot be made using low pass RC circuit?
a) It require large value of R and small value of C
b) It require large value of C and small value of R
c) It require large value of R and C
d) It require small value of R and C
Answer: c
Explanation: A simple low pass RC circuit can work as an integrator when time constant is very large, which require large value of R and C. Due to practical limitations , the R and C cannot be made infinitely large.

4. How a perfect integration is achieved in op-amp?
a) Infinite gain
b) Low input impedance
c) Low output impedance
d) High CMRR
Answer: a
Explanation: In an op-amp integrator the effective input capacitance becomes $C_F\times(1-A_v)$. Where A_v is the gain of op-amp. The gain is infinite for ideal op-amp. So, effective time constant of the op-amp integrator becomes very large which results in perfect integration.

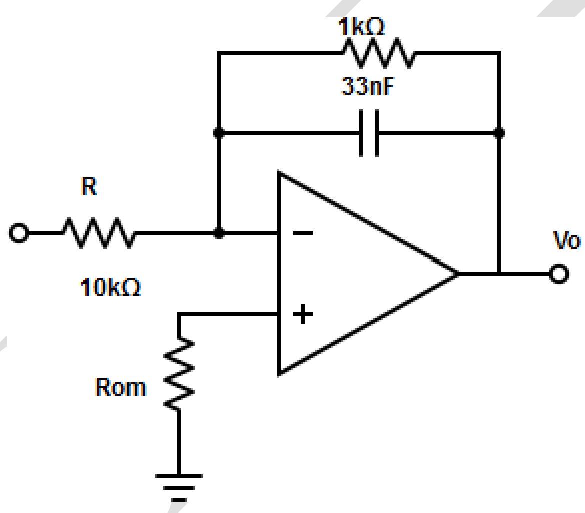
5. The op-amp operating in open loop result in output of the amplifier to saturate at a voltage
a) Close to op-amp positive power supply
b) Close to op-amp negative power supply

c) Close to op-amp positive or negative power supply
d) None of the mentioned
Answer: c
Explanation: In practice, the output of op-amp never becomes infinite rather the output of the op-amp saturate at a voltage close to op-amp positive or negative power supply depending on the polarity of the input dc signal.

6. The frequency at which gain is 0db for integrator is
a) $f=1/(2\pi R_F C_F)$
b) $f=1/(2\pi R_1 C_F)$
c) $f=1/(2\pi R_1 R_1)$
d) $f=(1/2\pi)\times(R_F/R_1)$
Answer: b
Explanation: The frequency at which the gain of the integrator becomes zero is $f=1/(2\pi R_1 C_F)$.

7. Why practical integrator is called as lossy integrator?
a) Dissipation power
b) Provide stabilization
c) Changes input
d) None of the mentioned
Answer: d
Explanation: To avoid saturation problems, the feedback capacitor is shunted by a feedback resistance(R_F). The parallel combination of R_F and C_F behave like a practical capacitor which dissipates power. For this reason, practical integrator is called as a lossy integrator.

8. Determine the lower frequency limit of integration for the circuit given below.



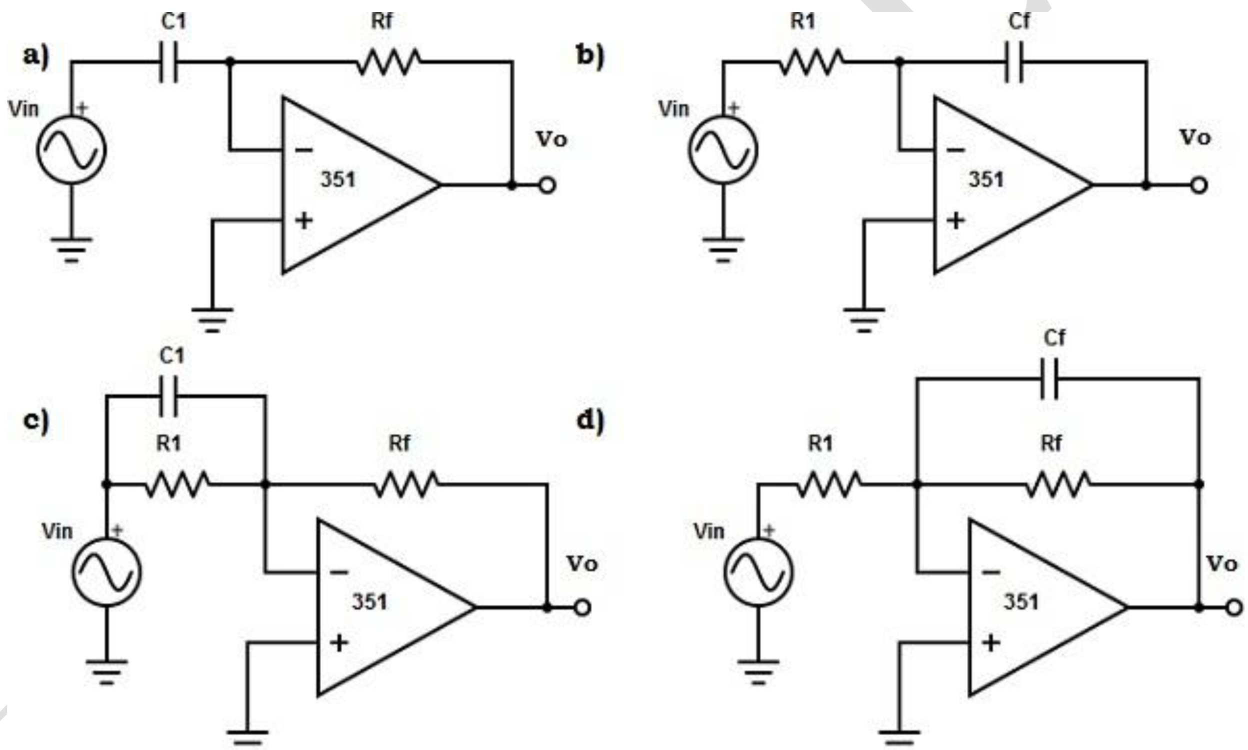
a) 43.43kHz
b) 4.82kHz
c) 429.9kHz
d) 4.6MHz
Answer: b

Explanation: The lower frequency limit of integration, $f = 1/(2\pi R_F C_F) = 1/(2\pi \times 1k\Omega \times 33nF) = 4.82kHz$.

Differentiator

1. Differentiation amplifier produces
a) Output waveform as integration of input waveform
b) Input waveform as integration of output waveform
c) Output waveform as derivative of input waveform
d) Input waveform as derivative of output waveform
Answer: c
Explanation: Differentiation amplifier or differentiator is a circuit that performs mathematical operation of differentiation and produce output waveform as a derivative of input waveform.

2. Find out the differentiator circuit from the given circuits?



Answer: a
Explanation: The differentiator is constructed from basic inverting amplifier by replacing the input resistor R_1 by replacing a capacitor C_1.

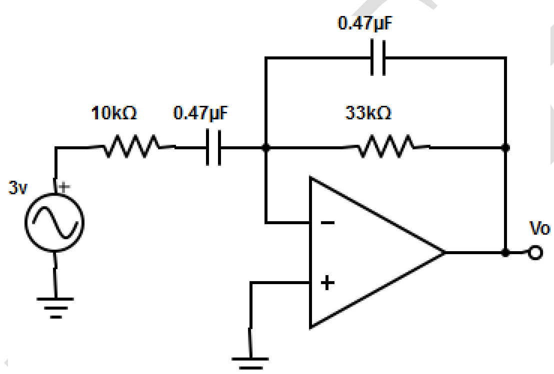
3. Determine the output voltage of the differentiator?
a) $V_O = R_F \times C_1 \times [dV_{in}/dt]$.
b) $V_O = -R_F \times C_1 \times [dV_{in}/dt]$.
c) $V_O = R_F \times C_F \times [dV_{in}/dt]$.

d) None of the mentioned
Answer: b
Explanation: The output voltage is equal to the $R_F \times C_1$ times the negative instantaneous rate of change of the input voltage V_{in} with time.

4. which factor makes the differentiator circuit unstable?
a) Output impedance
b) Input voltage
c) Noise
d) Gain
Answer: d
Explanation: The gain of the differentiator circuit (R_F / XC_1) increases with increase in frequency at a rate of 20dB/decade. This makes the circuit unstable.

5. The increase in the input frequency of the differentiation amplifier to input impedance creates
a) Component noise
b) External noise
c) Low frequency noise
d) High frequency noise
Answer: d
Explanation: The input impedance of the amplifier decreases with increase in frequency and make the circuit susceptible to high frequency noise such that noise can completely over ride differential output.

6. Calculate the gain limiting frequency for the circuit



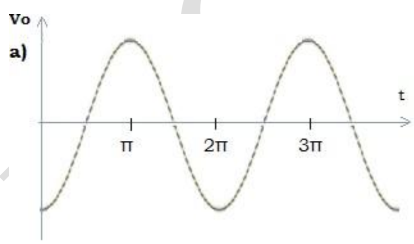
a) 15.64Hz
b) 23.356Hz
c) 33.89Hz
d) None of the mentioned
Answer: c
Explanation: The gain limiting frequency, $f_b = 1/(2\pi \times R_1 \times C_1)$.
$f_b = 1/(2\pi \times 10k\Omega \times 0.47\mu F) = 1/(2.9516 \times 10^{-2}) = 33.89Hz$.

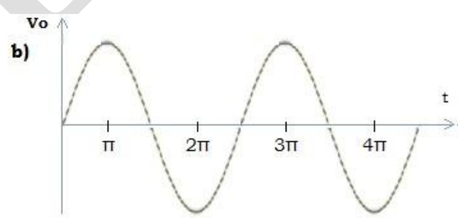
7. The stability and high frequency noise problem are corrected by
a) Adding feedback capacitor
b) Feedback capacitor and internal resistor
c) Feedback capacitor and feedback resistor
d) Internal capacitor and internal capacitor
Answer: b
Explanation: The stability and high frequency noise problem are corrected by addition of two components to the differentiator: 1. Internal resistor in series with internal capacitor and 2. Feedback capacitor shunts with feedback resistor.

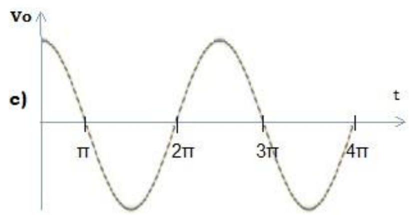
8. Select the order in which the frequency should be maintained to enhance the stability of differentiator? Where f_a -> Frequency at which gain =0 ; f_b -> Gain limit frequency ; f_c -> Unity gain bandwidth.
a) $f_a < f_b < f_c$
b) $f_a > f_b > f_c$
c) $f_b < f_c > f_a$
d) $f_b < f_c < f_a$
Answer: a
Explanation: The value of internal resistor and capacitor and feedback resistor and capacitor of the differentiator values should be selected such that $f_a < f_b < f_c$ to make the circuit more stable.

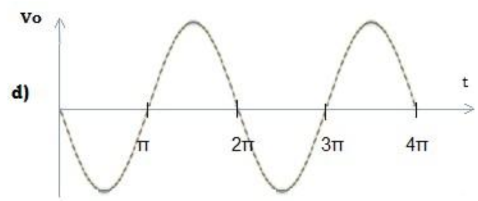
9. Which application use differentiator circuit?
a) None of the mentioned
b) FM modulators
c) Wave generators
d) Frequency Shift keying
Answer: b
Explanation: The differentiators are used in FM modulator as a rate of change detector.

10. A sine wave of $1v_{peak}$ at 1000Hz is applied to a differentiator with the following specification: R_F =1kΩ and C_1=0.33μF, find the output waveform?







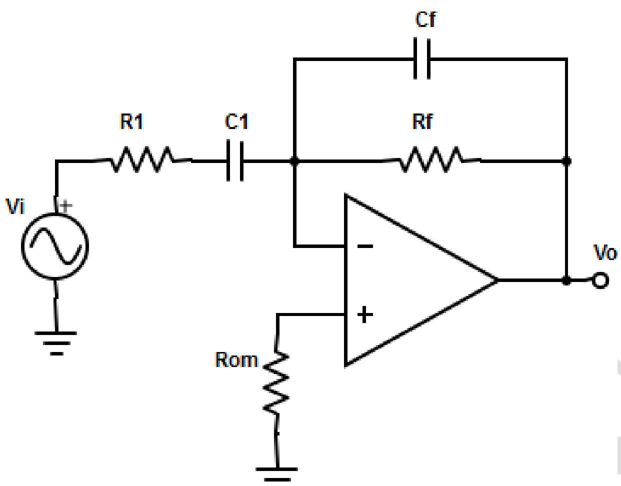


Answer: a
Explanation: Given, $V_{in} = V_p \times \sin\omega t = \sin(2\pi \times 1000)t$

The output of differentiator $V_o = -R_F \times C_1 \times (dV_{in}/dt) = (1k\Omega) \times (0.33\mu F) \times d[\sin 2\pi \times 1000t]/dt$
$= -3.3 \times 10^{-4} \times 2\pi \times 1000 \times [\cos 2\pi(1000)t] = -2.07 \times [\cos 2\pi(1000)t]$.

11. Choose the value of R_F and C for a 5kHz input signal to obtain good differentiation.
a) $R_F = 1.6 \times 10^3 \Omega$, $C_1 = 33 \times 10^{-6}F$
b) $R_F = 1.6 \times 10^3 \Omega$, $C_1 = 0.47 \times 10^{-6}F$
c) $R_F = 1.6 \times 10^3 \Omega$, $C_1 = 47 \times 10^{-6}F$
d) $R_F = 1.6 \times 10^3 \Omega$, $C_1 = 10 \times 10^{-6}F$

12. Determine the transfer function for the practical differentiator



a) $V_o(s) / V_1(s) = -S \times R_F \times C_1/(1+R_1 \times C_1)^2$
b) $V_o(s) / V_1(s) = -S \times R_F \times C_1/(1+R_F \times C_1)^2$
c) $V_o(s) / V_1(s) = -S \times R_F \times C_1/(1+R_1 \times C_F)^2$
d) None of the mentioned
Answer: a
Explanation: The transfer function for the circuit,
$V_o(s) / V_1(s) = -S \times R_F \times C_1/\{[1+(R_F C_F)] \times [1+(S \times R_1 \times C_1)]\}$.
In a practical differentiator, $R_F C_F = R_1 C_1$
$\Rightarrow V_o(s) / V_1(s) = -SR_F \times C_1/(1+SR_F \times C_F)^2$ or $V_o(s) / V_1'(s) = -S \times R_F \times C_1/(1+R_1 \times C_1)^2$.

Active Filters

1. An electrical filter is a
a) Phase-selective circuit
b) Frequency-selective circuit
c) Filter-selective circuit
d) None of the mentioned
Answer: b

Explanation: An electric filter is often a frequency selective circuit that passes a specified band of frequencies and blocks or alternates signal of frequencies outside this band.

2. Filters are classified as
a) Analog or digital
b) Passive or active
c) Audio or radio frequency
d) All of the mentioned
Answer: d
Explanation: Filters are classified based on the design technique (analog or digital), elements used for construction (active or passive) and operating range (audio or radio frequency).

3. Why inductors are not preferred for audio frequency?
a) Large and heavy
b) High power dissipation
c) High input impedance
d) None of the mentioned
Answer: a
Explanation: At audio frequencies, inductor becomes problematic, as the inductors become large, heavy and expensive.

4. The problem of passive filters is overcome by using
a) Analog filter
b) Active filter
c) LC filter
d) A combination of analog and digital filters
Answer: b
Explanation: The active filters enclose as a capacitor in the feedback loop and avoid using inductors, this way inductorless active filter are obtained.

5. What happens if inductors are used in low frequency applications?
a) Enhance inductor usage
b) No losses occurs
c) Degrades inductor performance
d) Low power dissipation
Answer: c
Explanation: For low frequency applications more number of turns of wire must be used, which in turn adds to the series resistance degrading inductor's performance.

6. Find out the incorrect statement about active and passive filters.
a) Gain is not attenuated in active filter
b) Passive filters are less expensive
c) Active filter does not cause loading of source
d) Passive filters are difficult to tune or adjust
Answer: b

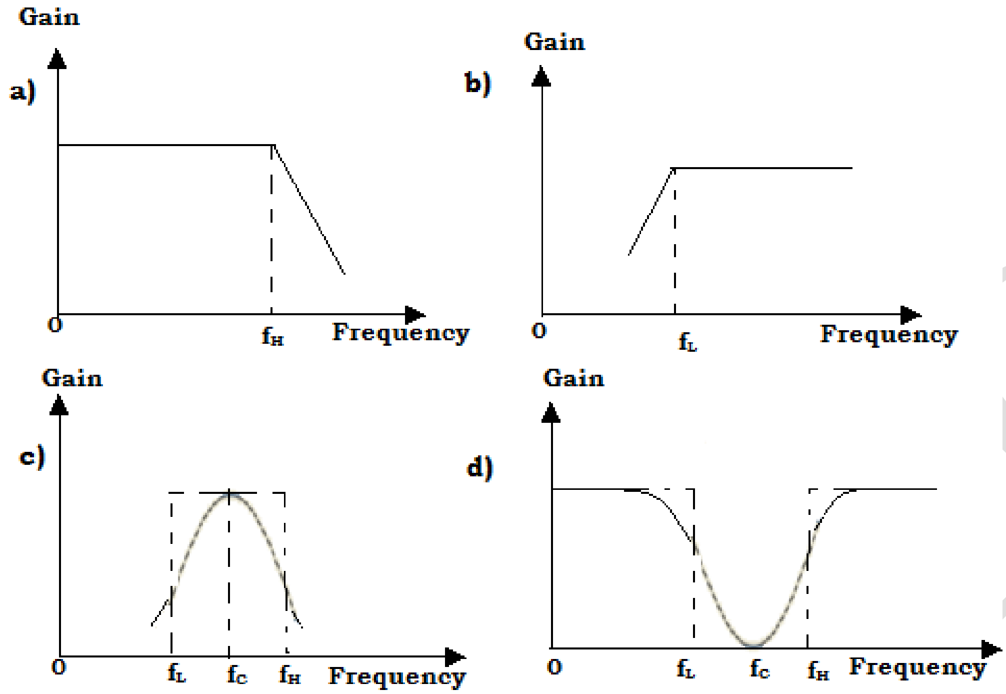
Explanation: Typically active filters are more economical than passive filters. This is because of the variety of cheaper op-amp and the absence of inductor’s.

7. What are the most commonly used active filters?
a) All of the mentioned
b) Low pass and High pass filters
c) Band pass and Band reject filters
d) All-pass filters
Answer: a
Explanation: All the mentioned filters use op-amp as active element and capacitors & resistors as passive elements.

8. Choose the op-amp that improves the filter performance.
a) µA741
b) LM318
c) LM101A
d) MC34001
Answer: b
Explanation: LM318 is a high speed op-amp that improves the filter’s performance through increased slew rate and higher unity gain-bandwidth.

9. Ideal response of filter takes place in
a) Pass band and stop band frequency
b) Stop band frequency
c) Pass band frequency
d) None of the mentioned
Answer: c
Explanation: The ideal response indicates the practical filter response and it lies within the pass band frequencies.

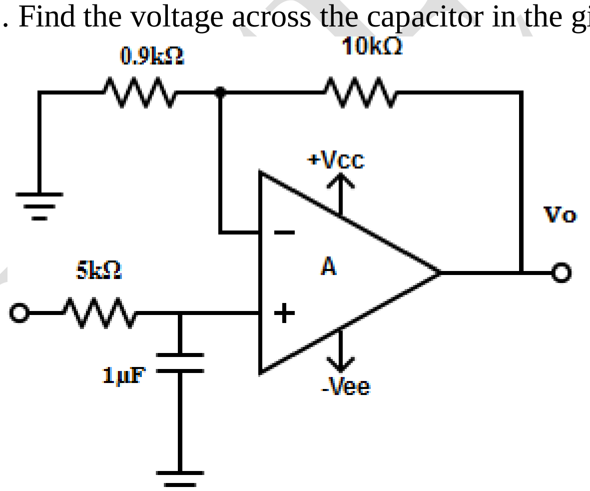
10. Find out the low pass filter from the given frequency response characteristics.



Answer: a
Explanation: A low pass filter has a constant gain from 0Hz to high cut-off frequency f_H.

First Order Low Pass Butterworth Filter

1. Find the voltage across the capacitor in the given circuit

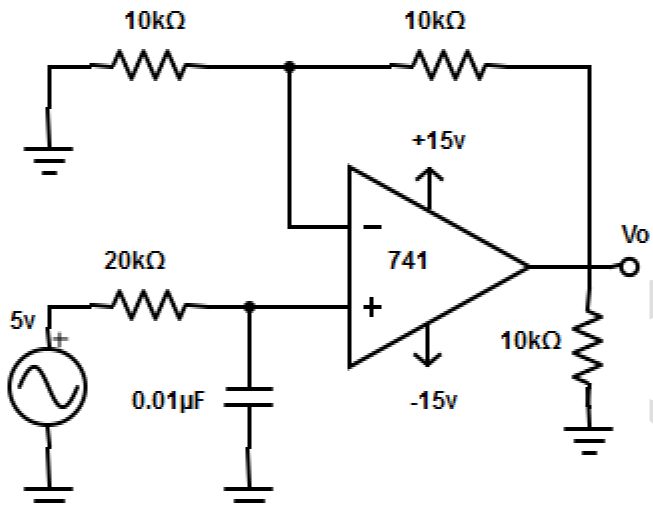


a) $V_O = V_{in}/(1+0.0314jf)$
b) $V_O = V_{in} \times (1+0.0314jf)$
c) $V_O = V_{in}+0.0314jf/(1+jf)$
d) None of the mentioned

Answer: a
Explanation: The voltage across the capacitor, $V_O = V_{in}/(1+j2\pi fR_C)$
=> $V_O = V_{in}/(1+j2\pi\times5k\times1\mu F\times f)$
=> $V_O = V_{in}/(1+0.0314jf)$.

2. Find the complex equation for the gain of the first order low pass butterworth filter as a function of frequency.
a) $A_F/[1+j(f/f_H)]$.
b) $A_F/\sqrt{[1+j(f/f_H)^2]}$.
c) $A_F\times[1+j(f/f_H)]$.
d) None of the mentioned
Answer: a
Explanation: Gain of the filter, as a function of frequency is given as $V_O/V_{in}=A_F/(1+j(f/f_H))$.

3. Compute the pass band gain and high cut-off frequency for the first order high pass filter.



a) $A_F=11$, $f_H=796.18Hz$
b) $A_F=10$, $f_H=796.18Hz$
c) $A_F=2$, $f_H=796.18Hz$
d) $A_F=3$, $f_H=796.18Hz$
Answer: c
Explanation: The pass band gain of the filter, $A_F=1+(R_F/R_1)$
$\Rightarrow A_F=1+(10k\Omega/10k\Omega)=2$. The high cut-off frequency of the filter, $f_H=1/2\pi RC$
$=1/(2\pi\times20k\Omega\times0.01\mu F)=1/1.256\times10^{-3}=796.18Hz$.

4. Match the gain of the filter with the frequencies in the low pass filter

Frequency	Gain of the filter
1. $f < f_H$	i. $V_O/V_{in} \cong A_F/\sqrt{2}$
2. $f=f_H$	ii. $V_O/V_{in} \leq A_F$
3. $f>f_H$	iii. $V_O/V_{in} \cong A_F$

a) 1-i,2-ii,3-iii
b) 1-ii,2-iii,3-i
c) 1-iii,2-ii,3-i
d) 1-iii,2-i,3-ii
Answer: d
Explanation: The mentioned answer can be obtained, if the value of frequencies are substituted in the gain magnitude equation $|(V_o/V_{in})|=A_F/\sqrt{(1+(f/f_H)^2)}$.

5. Determine the gain of the first order low pass filter if the phase angle is 59.77^o and the pass band gain is 7.
a) 3.5
b) 7
c) 12
d) 1.71
Answer: a
Explanation: Given the phase angle, $\varphi =-\tan^{-1}(f/f_H)$
$\Rightarrow f/f_H=- \varphi\tan(\varphi) = -\tan(59.77^o)$
$\Rightarrow f/f_H= -1.716$.
Substituting the above value in gain of the filter, $|(V_O/V_{in})| = A_F/\sqrt{(1+(f/f_H)^2)} =7/\sqrt{[1+(-1.716)^2)]}$
$=7/1.986$
$\Rightarrow|(V_O/V_{in})|=3.5$.

6. In a low pass butterworth filter, the condition at which $f=f_H$ is called
a) Cut-off frequency
b) Break frequency
c) Corner frequency
d) All of the mentioned
Answer: d
Explanation: The frequency, $f=f_H$ is called cut-off frequency, because the gain of the filter at this frequency is down by 3dB from 0Hz. Cut-off frequency is also called as break frequency, corner frequency or 3dB frequency.

7. Find the High cut-off frequency if the pass band gain of a filter is 10.
a) 70.7Hz
b) 7.07kHz
c) 7.07Hz
d) 707Hz
Answer: c
Explanation: High cut-off frequency of a filter, $f_H=0.707\times A_F =0.707\times10$
$\Rightarrow f_H=7.07$Hz.

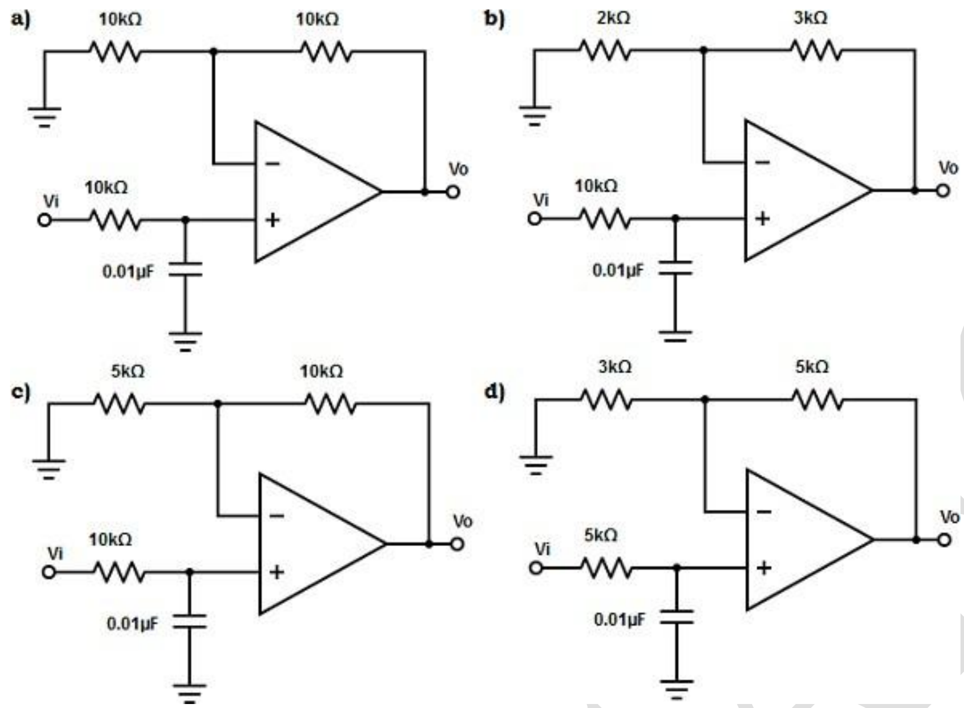
8. To change the high cutoff frequency of a filter. It is multiplied by R or C by a ratio of original cut-off frequency known as
a) Gain scaling
b) Frequency scaling
c) Magnitude scaling

d) Phase scaling
Answer: b
Explanation: Once a filter is designed, it may sometimes be a need to change it's cut-off frequency. The procedure used to convert an original cut-off frequency f_H to a new cut-off frequency is called frequency scaling.

9. Using the frequency scaling technique, convert 10kHz cut-off frequency of the low pass filter to a cutoff frequency of 16kHz.(Take C=0.01µF and R=15.9kΩ)
a) 6.25kΩ
b) 9.94kΩ
c) 16kΩ
d)1.59kΩ
Answer: b
Explanation: To change a cut-off frequency from 10kHz to 16kHz,multiply 15.9kΩ resistor.
[Original cut-off frequency/New cut-off frequency] =10kHz/16kHz =0.625.
∴ R =0.625×15.9kΩ =9.94kΩ. However 9.94kΩ is not a standard value. So, a potentiometer of 10kΩ is taken and adjusted to 9.94kΩ.

10. Find the difference in gain magnitude for a filter ,if it is the response obtained for frequencies f_1=200Hz and f_2=3kHz. Specification: A_F=2 and f_H=1kHz.
a) 4.28 dB
b) 5.85 dB
c) 1.56 dB
d) None of the mentioned
Answer: c
Explanation: When f_1=200Hz, $V_O(1)/V_{in} = A_F/\sqrt{[1+(f/f_H)^2]} = 2/\sqrt{[1+(200/1kHz)^2]} = 2/1.0198$.
=> $V_O(1)/V_{in} = 1.96$
=>$20\log|(V_O/V_{in})| = 5.85dB$.
When f=700Hz, $V_O(2)/V_{in} = 2/\sqrt{[1+(700/1kHz)^2]} = 2/1.22 = 1.638$.
=> $V_O(2)/V_{in} = 20\log|(V_O/V_{in}| = 20\log(1.638) = 4.28$.
Therefore, the difference in the gain magnitude is given as $V_O(1)/V_{in} - V_O(2)/V_{in}$ =5.85-4.28 =1.56 dB.

11. Design a low pass filter at a cut-off frequency 1.6Hz with a pass band gain of 2.



Answer: a
Explanation: From the answer, it is clear that all the C values are the same . Therefore, c= 0.01µF
Given, f_H = 1kHz,
=> R= $1/(2\pi Cf_m) = 1/2\pi\times0.01\mu F\times1kHz$
R= 9.9kΩ ≅ 10kΩ. Since the pass band gain is 2.
=> $2=1+ (R_F/R_1)$. Therefore, R_F and R_1 must be equal.

Sine Wave Oscillator

1. What is Barkhausen criterion for oscillation?
a) Aß > 1
b) Aß < 1
c) Aß = 1
d) Aß ≠ 1
Answer: c
Explanation: The Barkhausen criterion for oscillation is Aß = 1.
Where, A-> gain of amplifier and ß-> transfer ratio.

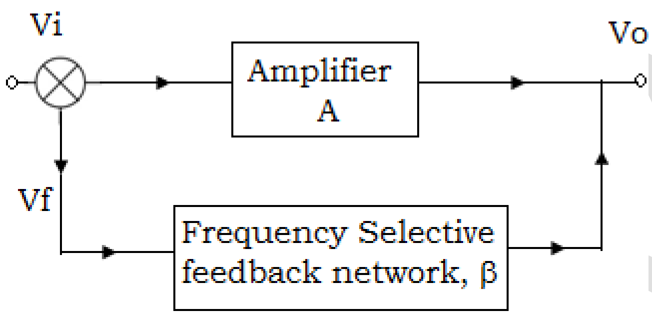
2. At what condition the output signal can be continuously obtained from input signal?
a) When the product of input voltage and feedback voltage is equal to 1
b) When the product of amplifier gain and transfer ratio is equal to 1
c) When the product of feedback voltage and transfer ratio is equal to 1
d) When the product of amplifier gain and input voltage is equal to 1
Answer: b
Explanation: When Aß=1, the feedback signal will be equal to the input signal. At this condition,

the circuit will continue to provide output, even if the external signal is disconnected. This is because the amplifier cannot distinguish between external signal and signal from the feedback circuit. Thus, output signal is continuously obtained.

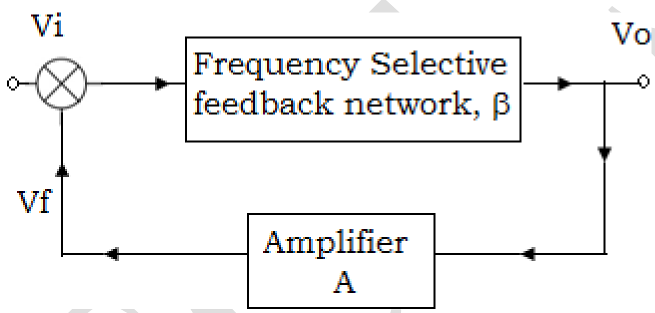
3. An oscillator is a type of
a) Feedforward amplifier
b) Feedback amplifier
c) Waveform amplifier
d) RC amplifier
Answer: b
Explanation: An oscillation is a type of feedback amplifier in which a part of output is fed back to the input via a feedback circuit.

4. Find the basic structure of feedback oscillator.

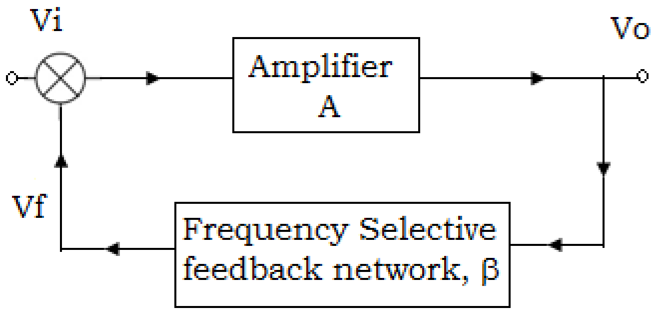
a)



b)



c)



d) None of the mentioned
Answer: c
Explanation: The above mentioned diagram is the basic structure of feedback oscillator. It consists of an amplifier, to the external input (v_i) is applied and it have a feedback network from which the feedback signal (v_f) is obtained.

5. What is the condition to achieve oscillations?
a) |Aß|=1
b) ∠Aß=0^o
c) ∠Aß=multiples of 2π
d) All the mentioned
Answer: d
Explanation: All the conditions should be simultaneously satisfied to achieve oscillations.

6. What happens if |Aß|<1
a) Oscillation will die down
b) Oscillation will keep on increasing
c) Oscillation remains constant
d) Oscillation fluctuates
Answer: a
Explanation: If |Aß| becomes less than unity, the feedback signal goes on reducing in each feedback cycle and oscillation will die down eventually.

7. How sustained oscillation can be achieved?
a) Maintaining |Aß| slightly greater than unity
b) Maintaining |Aß| equal to unity
c) Due to non-linearity of transistor
d) Due to use of feedback network
Answer: c
Explanation: When |Aß| is kept slightly greater than unity the signal, however, cannot go on increasing and get limited due to non-linearity of the device (that is transistor enters into saturation). Thus, it is the non-linearity of the transistor because of which the sustained oscillation can be achieved.

8. Why it is difficult to maintain Barkhausen condition for oscillation?
a) Due to variation in temperature
b) Due to variation in supply voltage

c) Due to variation in components life time
d) All of the mentioned
Answer: d
Explanation: The Barkhausen condition |Aß|=1 is usually difficult to maintain in the circuit as the value of A and ß vary due to temperature variations, aging of components, change of supply voltage etc.

9. Name the type of noise signal present in the oscillation?
a) Schmitt noise
b) Schottky noise
c) Saturation noise
d) None of the mentioned
Answer: b
Explanation: Schottky noise is the noise signal always present at the input of the transistor due to variation in the carrier concentration.

10. A basic feedback oscillator is satisfying the Barkhausen criterion. If the ß value is given as 0.7072, find the gain of basic amplifier?
a) 2.1216
b) 0.7072
c) 1
d) 1.414
Answer: d
Explanation: Barkhausen criterion for oscillation is given as Aß=1
=> A=1/ ß = 1/0.7072 = 1.414.

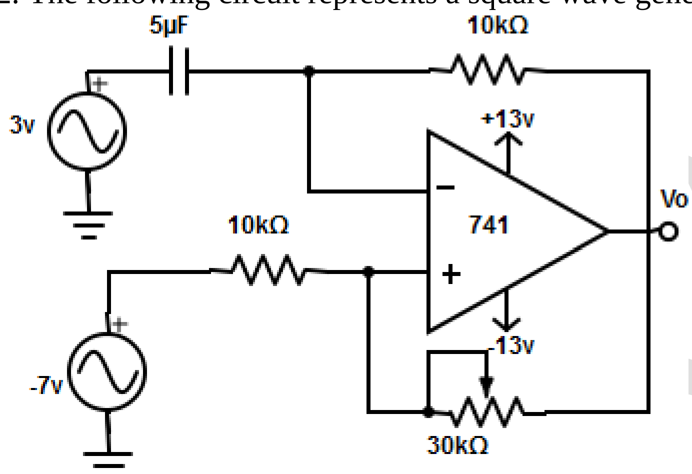
11. The feedback signal of basic sine wave oscillator is given as
a) V_f = Aß ×V_o
b) V_f = Aß ×V_i
c) V_f = Aß × (V_o/ V_i)
d) V_f = Aß × (V_i/ V_o)
Answer: b
Explanation: The feedback signal of an oscillator is given as the product of external applied signal & the loop gain of the system.
=> V_f= Aß ×V_i.

12. Express the requirement for oscillation in polar form
a) Aß =$1\angle 360^o$
b) Aß =$1\angle 90^o$
c) Aß =$1\angle \pi^o$
d) Aß =$1\angle 270^o$
Answer: a
Explanation: There are two requirements for oscillation
1. The magnitude of Aß=1
2. The total phase shift of Aß=0^o or 360^o.

Square Wave Generator

1. How are the square wave output generated in op-amp?
a) Op-amp is forced to operate in the positive saturation region
b) Op-amp is forced to operate in the negative saturation region
c) Op-amp is forced to operate between positive and negative saturation region
d) None of the mentioned
Answer: c
Explanation: Square wave outputs are generated where the op-amp is forced to operate in saturated region, that is, the output of the op-amp is forced to swing repetitively between positive saturation, $+V_{sat}$ and negative saturation, $-V_{sat}$.

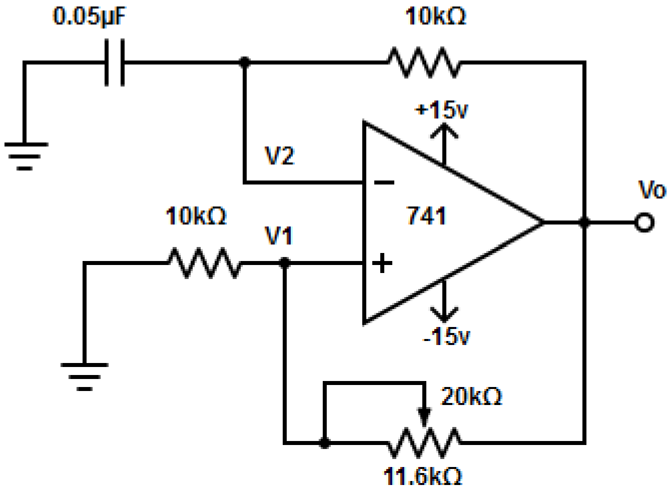
2. The following circuit represents a square wave generator. Determine its output voltage



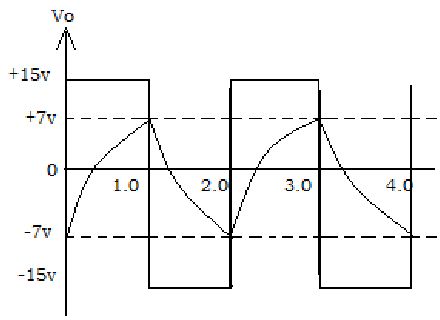
a) -13 v
b) +13 v
c) ± 13 v
d) None of the mentioned
Answer: a
Explanation: The differential output voltage $V_{id} = V_{in1} – V_{in2}= 3-7v = -4v$.
The output of the op-amp in this circuit depends on polarity of differential voltage $V_0= -V_{sat} \cong -V_{ee} = -13$ v.

3. Determine the expression for time period of a square wave generator
a) $T= 2RC \ln\times[(R_1+ R_2) / (R_2)]$.
b) $T= 2RC \ln\times[(2R_1+ R_2) / (R_2)]$.
c) $T= 2RC \ln\times[(R_1+ 2R_2) / (R_2)]$.
d) $T= 2RC \ln\times[(R_1+ R_2) / (2 R_2)]$.
Answer: b
Explanation: The time period of the output waveform for a square wave generator is $T= 2RC \ln\times[(2R_1+ R_2)/(R_2)]$.

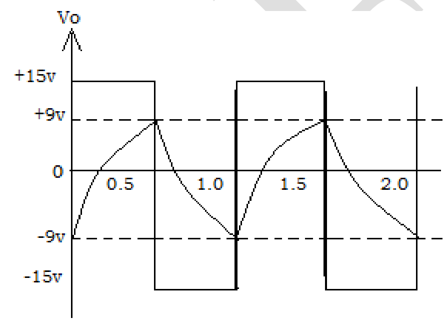
4. Determine capacitor voltage waveform for the circuit



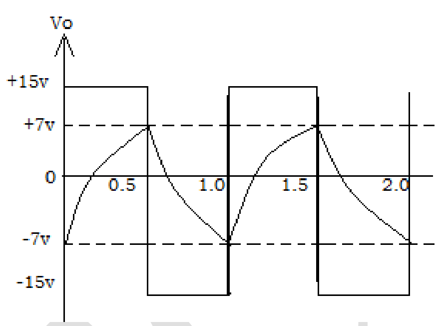
a)



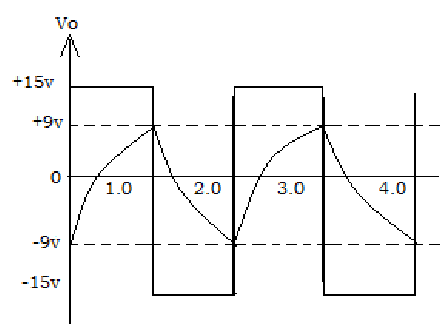
b)



c)



d)



Answer: c

Explanation: When the op-amp output voltage is at negative saturation, $V_1 = [(R_1) / (R_1 + R_2)] \times (-V_{sat}) = [10k\Omega / (10\ k\Omega + 11.6\ k\Omega)] \times (-15v) = -7v$.

Similarly, when the op-amp's output voltage is at positive saturation, $V_1 = [(R_1) / (R_1 + R_2)] \times (+V_{sat}) = [10k\Omega / (10\ k\Omega + 11.6\ k\Omega)] \times (+15v) = +7v$

The time period of the output waveform, $T = 2RC \ln \times [(2R_1 + R_2) / (R_2)] = 2 \times 10k\Omega \times 0.05\ \mu F \times \ln (2 \times 10k\Omega + 11.6k\Omega) / 11.6k\Omega] = 1 \times 10^{-3} \times \ln 2.724 = 1ms$.

The voltage across the capacitor will be a triangular wave form.

5. What will be the frequency of output waveform of a square wave generator if $R_2 = 1.16 R_1$?

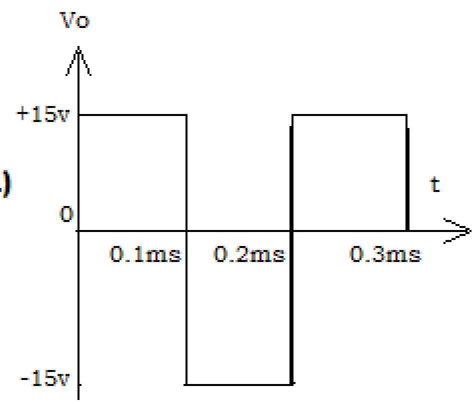
a) $f_o = (1/2RC)$

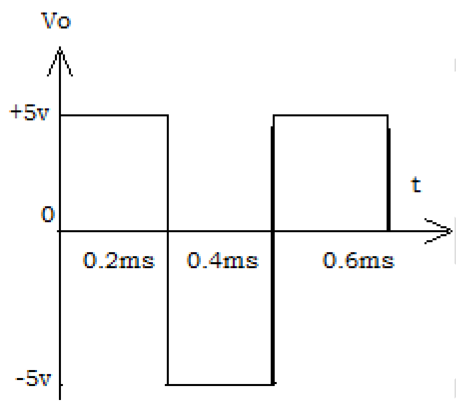
b) $f_o = (\ln/2RC)$

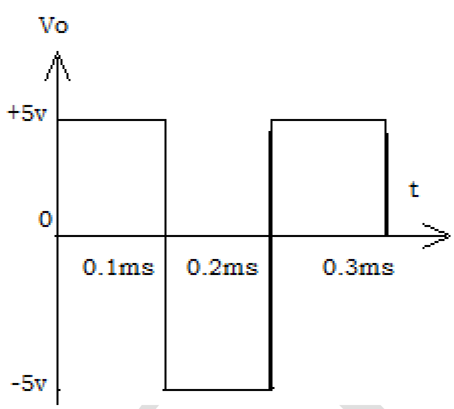
c) $f_o = (\ln /2 \times \sqrt{RC})$

d) $f_o = (\ln/\sqrt{(2\ RC)})$
Answer: b
Explanation: When $R_2 = 1.16\ R_1$, then $f_o = 1/2RC \times \ln[\ (2R_1 + R_2) / R_2] = 1/2RC \times \ln\ [(2R_1 + 1.161R_1)/\ (1.161R_1)] = 1/(\ 2RC \times \ln 2.700) = 1/2RC$.

6. What could be the possible output waveform for a free running multivibrator whose op-amp has a supply voltage of ±5v operating at 5khz?

a)


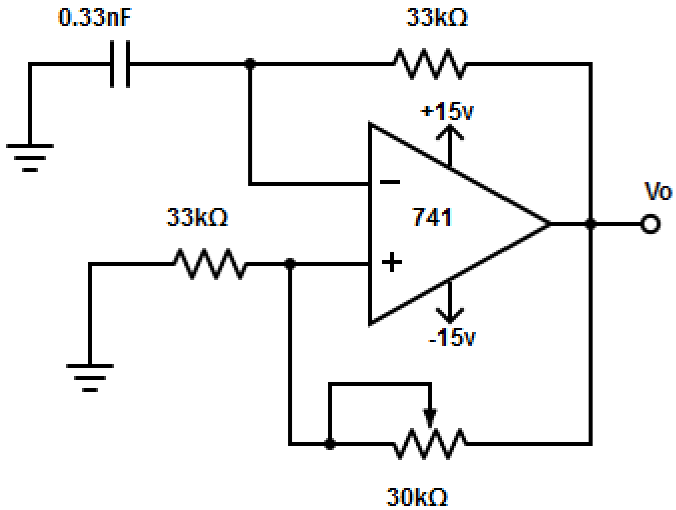
b)


c)


d) None of the mentioned

Answer: c
Explanation: In a free running multivibrator, the output is forced to swing repetitively between positive and negative saturation to produce square wave output. Therefore, $+V_{sat} \cong +V_{cc} = +5v$ and $-V_{sat} \cong -V_{cc} = -5v$.
=> Frequency= 5khz , f =1/t = 0.2ms.

7. Determine the output frequency for the circuit given below



a) 28.77 Hz
b) 31.97 Hz
c) 35.52 Hz
d) 39.47 Hz
Answer: d
Explanation: The output frequency $f_o = 1/2RC \times \ln [(2R_1 + R_2)/ R_2] = 1 / \{(2\times33k\Omega \times0.33\mu F)\times\ln[(2\times33k\Omega + 30k\Omega)/30k\Omega]\} = 1/ (0.02175\times\ln 32) = 39.47$ Hz.

8. The value of series resistance in the square wave generator should be 100kΩ or higher in order to
a) Prevent excessive differential current flow
b) Increase resistivity of the circuit
c) Reduce output offset voltage
d) All of the mentioned
Answer: a
Explanation: In practice, each inverting and non-inverting terminal needs a series resistance to prevent excessive differential current flow because the inputs of the op-amp are subjected to large differential voltages.

9. Why zener diode is used at the output terminal of square wave generator?
a) To reduce both output and capacitor voltage swing
b) To reduce output voltage swing
c) To reduce input voltage swing
d) To reduce capacitor voltage swing
Answer: b
Explanation: A reduced peak-peak output voltage swing can be obtained in the square wave generator by using back to back zener diodes at the output terminal.

10. A square wave oscillator has f_o =1khz. Assume the resistor value to be 10kΩ and find the capacitor value?
a) 3.9 µF

b) 0.3 μF
c) 2 μF
d) 0.05μF
Answer: d
Explanation: Let's take $R_2 = 1.16\ R_2$, therefore the output frequency $f_o = 1/2RC$
=> $C = 1/2Rf_o = 1/\ (2\times10k\Omega\times1khz) = 0.05\mu F$

Triangular and Sawtooth Wave Generator

1. How a triangular wave generator is derived from square wave generator?
a) Connect oscillator at the output
b) Connect Voltage follower at the output
c) Connect differential at the output
d) Connect integrator at the output
Answer: d
Explanation: The output waveform of the integrator is triangular, if its input is square wave. Therefore, a triangular wave generator can be obtained by connecting an integrator at the output of the square wave generator.

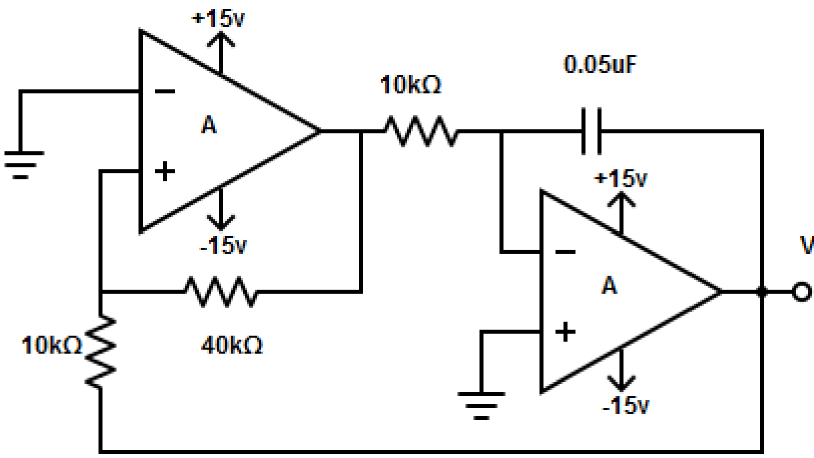
2. The increase in the frequency of triangular wave generator.
a) Ramp the amplitude of triangular wave
b) Increase the amplitude of triangular wave
c) Decrease the amplitude of triangular wave
d) None of the mentioned
Answer: a
Explanation: As the resistor value increase or decrease, the frequency of triangular wave will decrease or increase, respectively. Therefore, the amplitude of the triangular wave decreases with an increase in it frequency and vice verse.

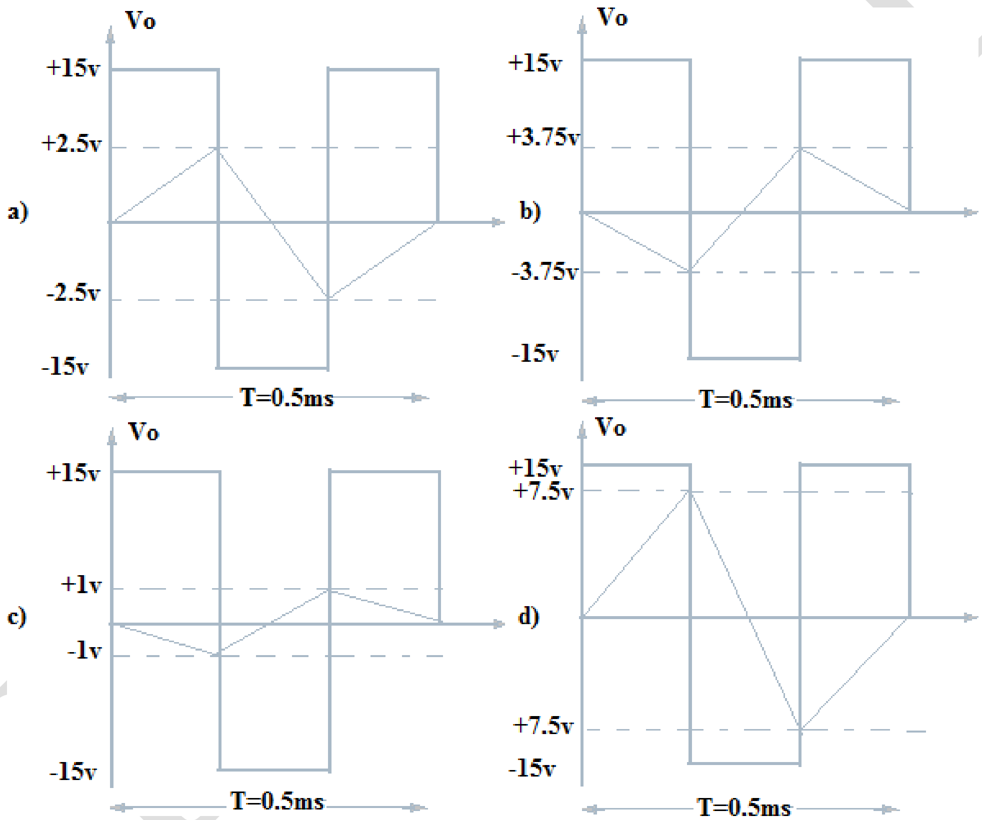
3. Which among the following op-amp is chosen for generating triangular wave of relatively higher frequency?
a) LM741 op-amp
b) LM301 op-amp
c) LM1458 op-amp
d) LM3530 op-amp
Answer: b
Explanation: The frequency of the triangular wave generator is limited by the slew rate of the op-amp. LM301 op-amp has a high slew rate.

4. What is the peak to peak (PP) output amplitude of the triangular wave?
a) $V_O(pp) = +V_{Ramp} + (-V_{Ramp})$
b) $V_O(pp) = -V_{Ramp} + (+V_{Ramp})$
c) $V_O(pp) = +V_{Ramp} - (-V_{Ramp})$
d) $V_O(pp) = -V_{Ramp} - (+V_{Ramp})$
Answer: c
Explanation: The peak to peak output waveform, $V_O(pp) = +V_{Ramp}-(-V_{Ramp})$

Where, – V_{Ramp} –> Negative going ramp ;
+ V_{Ramp}–> positive going ramp.

5. Determine the output triangular waveform for the circuit.





Answer: b
Explanation: The voltage at which A_1 switch from $+V_{sat}$ to $-V_{sat}$
=> $-V_{ramp} = (-R_2 / R_3) \times (+V_{sat})$
$= (-10k\Omega/40k\Omega) \times 15v = -3.75v$
Similarly, the voltage at which A_1 switch from $-V_{sat}$ to $+V_{sat}$
=> $+V_{ramp} = (-R_2 / R_3) \times (-V_{sat})$
$= 10k\Omega/40k\Omega \times 15v = 3.75v$

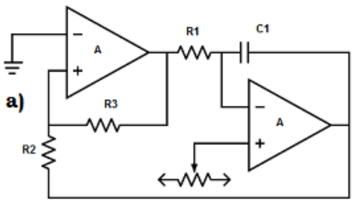
∴ Time period, $T = (4R_1C_1R_2) / R_3$
$= (4\times10k\Omega\times0.05\mu F\times10k\Omega) / 40k\Omega = 0.5$ ms.

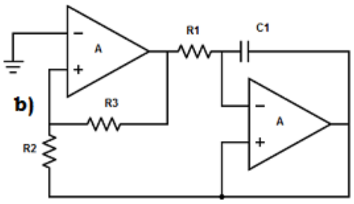
6. Find the capacitor value for a the output frequency, $f_o = 2kHz$ & $V_O(pp) = 7v$, in a triangular wave generator. The op-amp is 1458/741 and supply voltage = ±15v. (Take internal resistor=10kΩ)
a) 0.03nF
b) 30nF
c) 0.3nF
d) 3nF
Answer: d
Explanation: Given, $V_{sat} = 15v$
$\therefore V_O(pp) = (2R_2/R_3) \times V_{sat}$
$\Rightarrow R_2 = (V_O(pp) \times R_3) / (V_{sat}\times2) = [7/(2\times15)]\times R_3 = 0.233R_3$
$\because$ Internal resistor, $R_2 = R_1 = 10k\Omega$
$\Rightarrow R_3 = 0.233\times10k\Omega = 2.33k\Omega$.
So, the output frequency $f_O = R_3 / (4\times R_1 \times C_1\times R_2)$
$\Rightarrow 2khz = 2.33khz / (4\times10k\Omega \times10k\Omega\times C_1)$
$\Rightarrow C_1 = 2.33k\Omega / (8\times10^{-11}) = 2.9 \times10^{-9} \cong 3nF$.

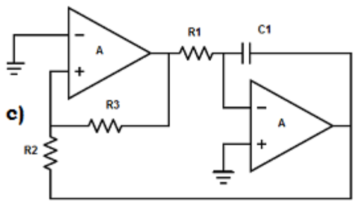
7. Triangular wave form has
a) Rise time < fall time
b) Rise time = fall time
c) Rise time ≥ fall time
d) None of the mentioned
Answer: b
Explanation: The triangular wave form has rise time of the triangular wave always equal to its fall time, that is, the same amount of time is required for the triangular wave to swing from $-V_{Ramp}$ to $+V_{Ramp}$ as from $+V_{Ramp}$ to $-V_{Ramp}$.

8. Output of an integrator producing waveforms of unequal rise and fall time are called
a) Triangular waveform
b) Sawtooth waveform
c) Pulsating waveform
d) Spiked waveform
Answer: b
Explanation: Sawtooth waveform has unequal rise and fall times. It may rise positively many times faster than it falls negatively or vice versa.

9. Find out the sawtooth wave generator from the following circuits.

a) 

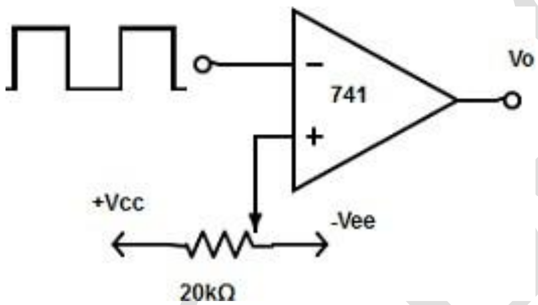
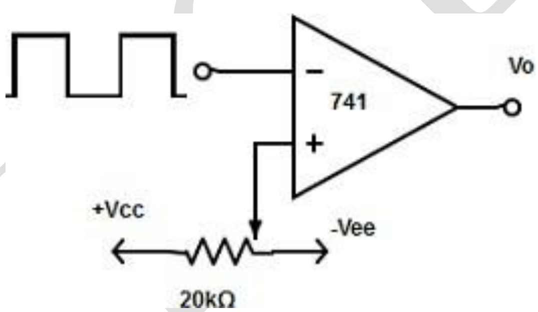
b) 

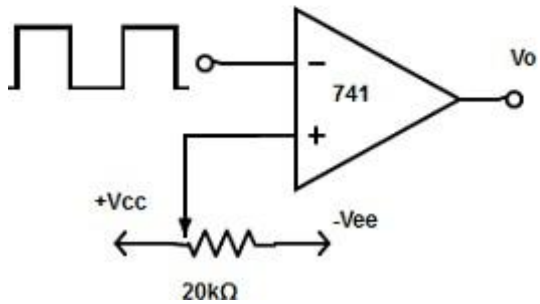
c) 

d) None of the mentioned

Answer: c
Explanation: The triangular wave generator can be converted into a sawtooth wave generator by inserting a variable dc voltage into the non-inverting terminal of the integrator.

10. Consider the integrator used for generating sawtooth wave form. Match the list I with the list II depending on the movement of wiper.

List-I	List-II
	Rise time =fall time (Triangular wave)
	Longer fall time and short rise time (Sawtooth wave)



Longer rise time and short fall time (Sawtooth wave)

a) 1-iii, 2-ii, 3-i
b) 1-i, 2-ii, 3-iii
c) 1-i, 2-iii, 3-ii
d) 1-ii, 2-iii, 3-i
Answer: c
Explanation: Depending on the duty cycle (movement of the wiper) the type of waveform is determined.